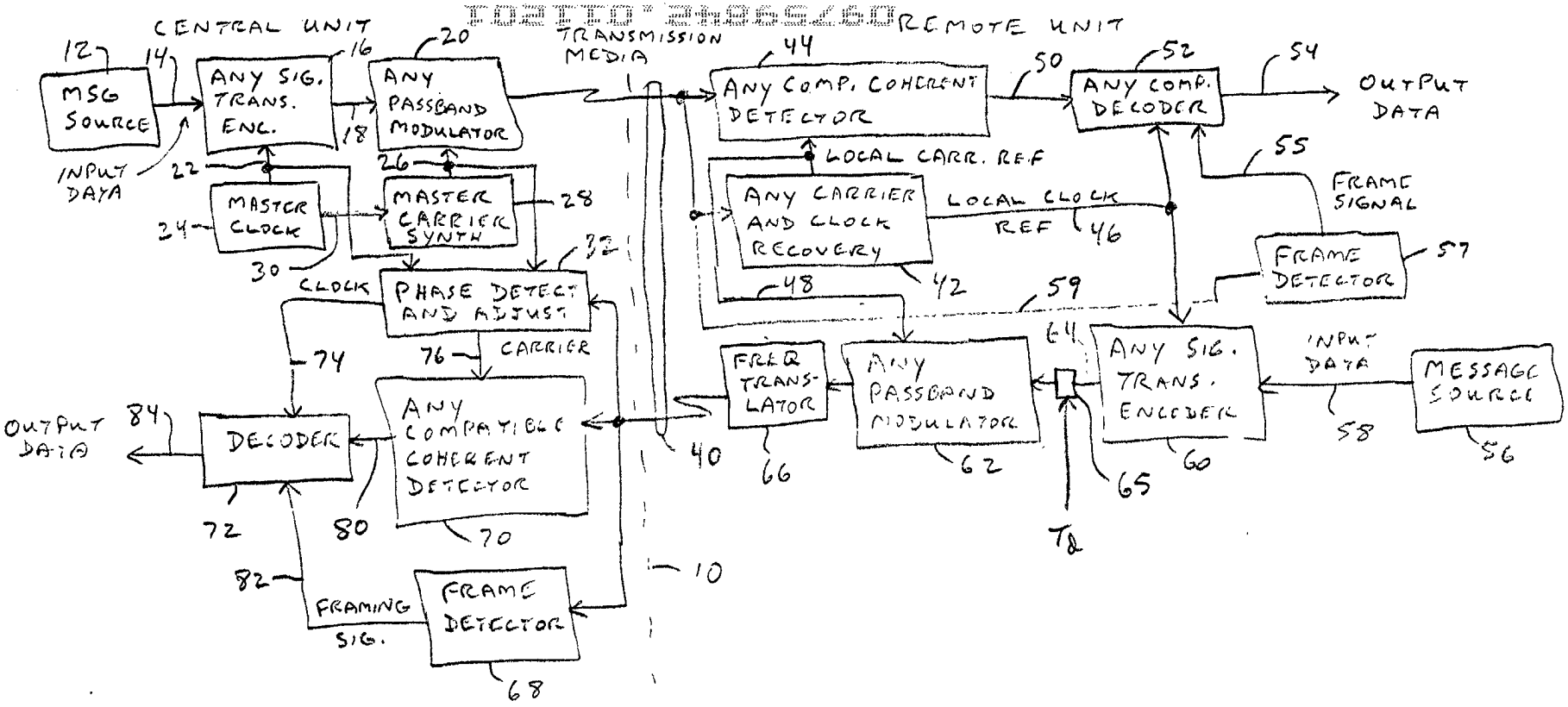


FIG. 1

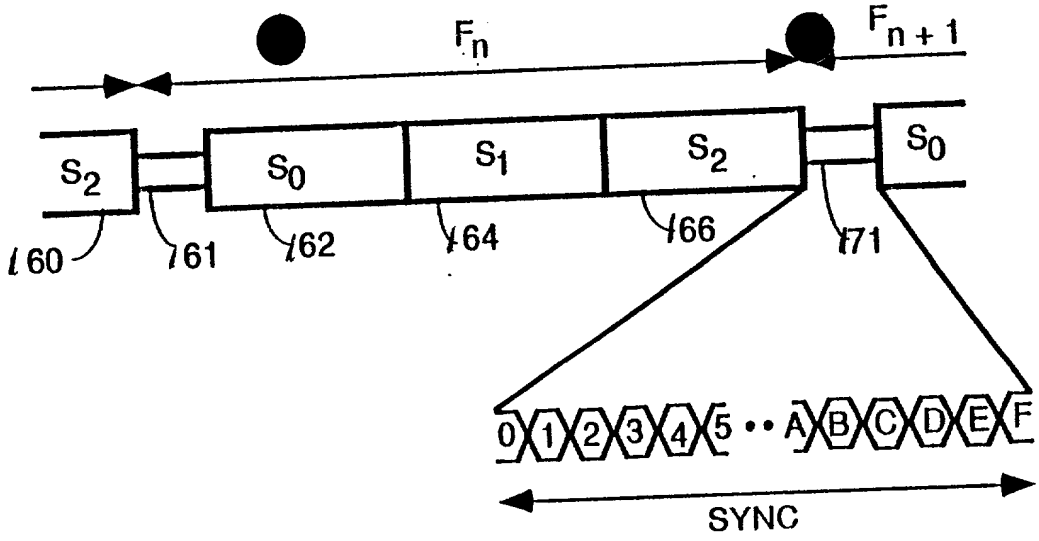

F_n
F_{n+1}
S_2
S_0
S_1
S_2
S_0
160
161
162
164
166
171
0 1 2 3 4 5 • • A B C D E F
SYNC

FIG. 2A

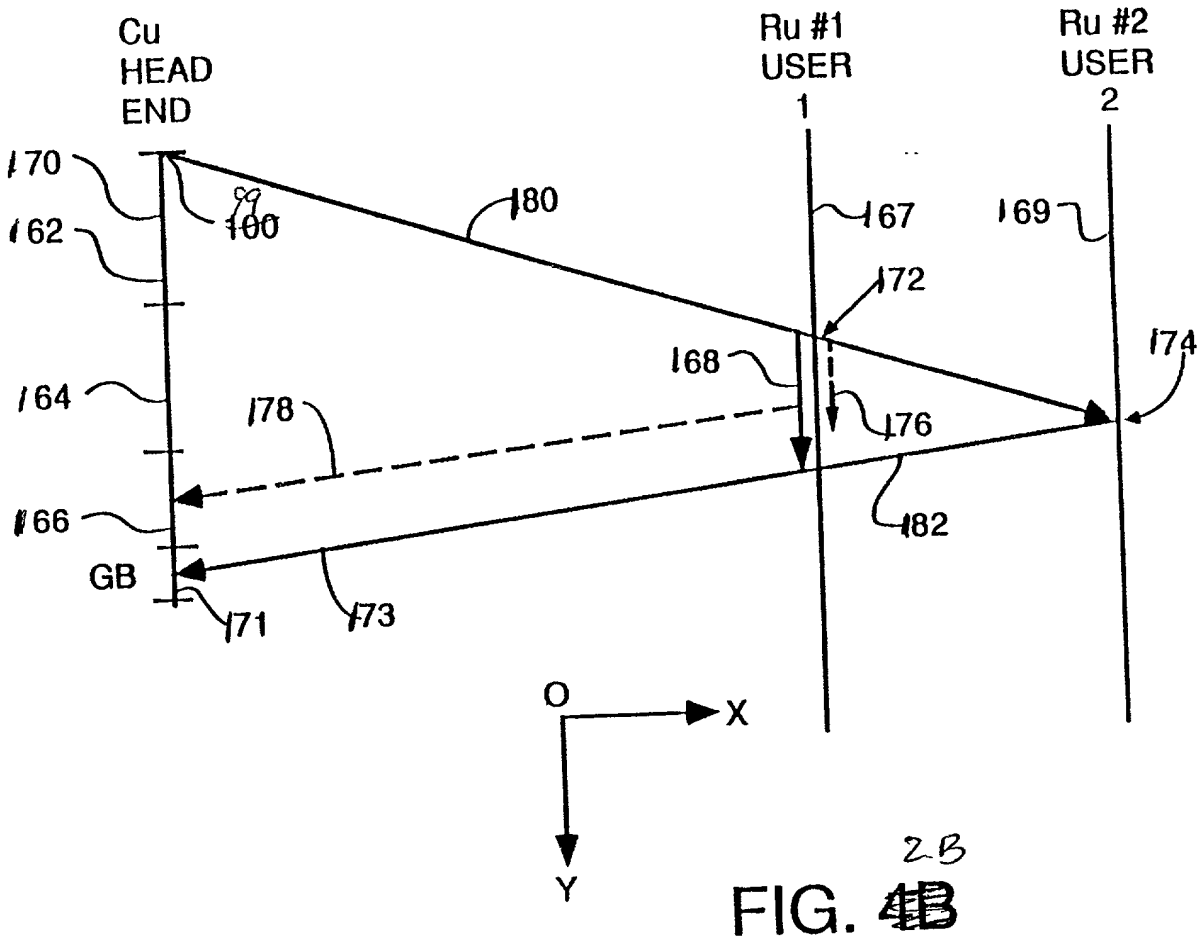

Cu
HEAD
END
Ru #1
USER
1
Ru #2
USER
2
170
162
164
166
GB
171
173
178
180
167
169
172
168
174
176
182
O
X
Y

FIG. 2B

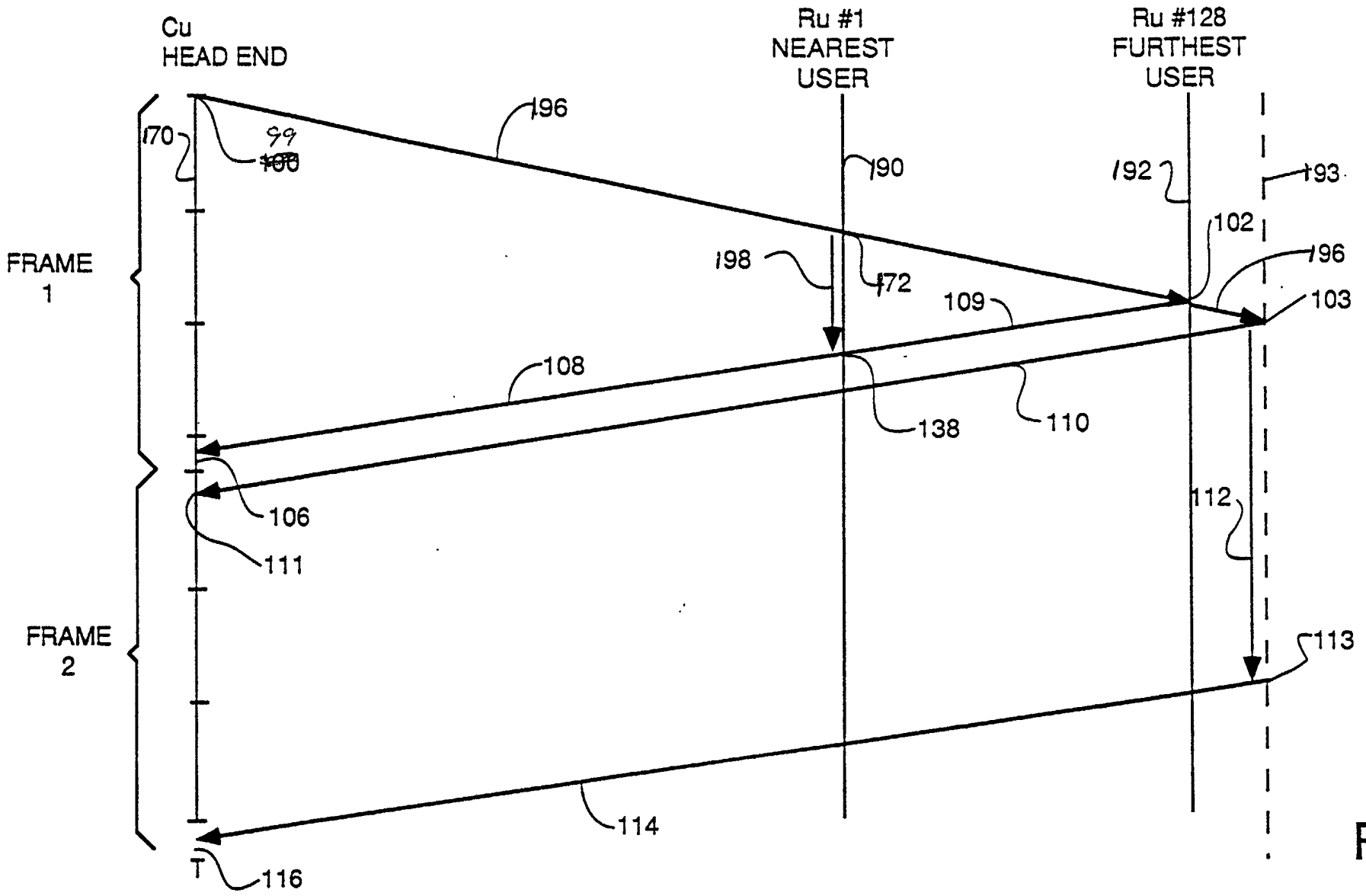


FIG. 5

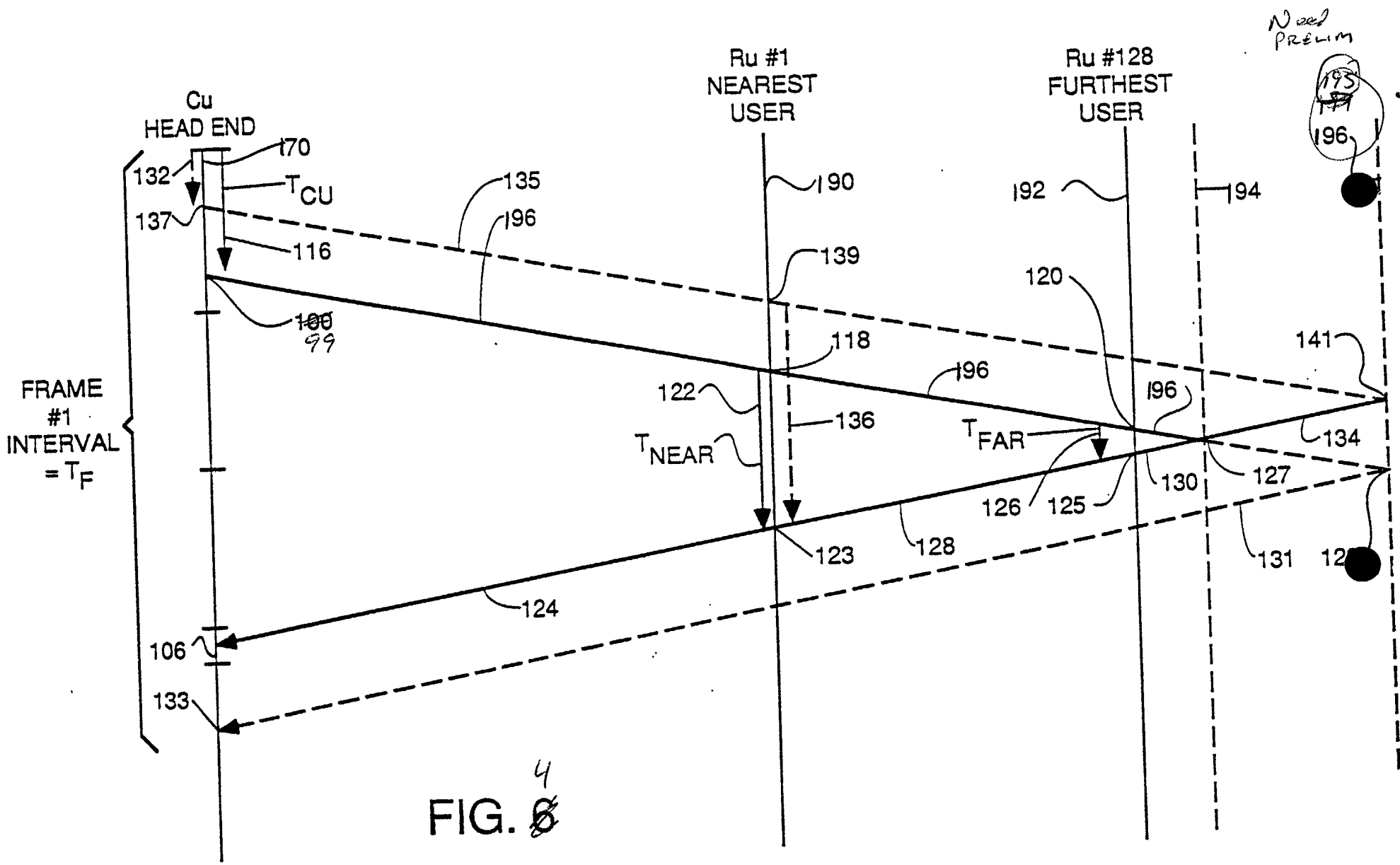
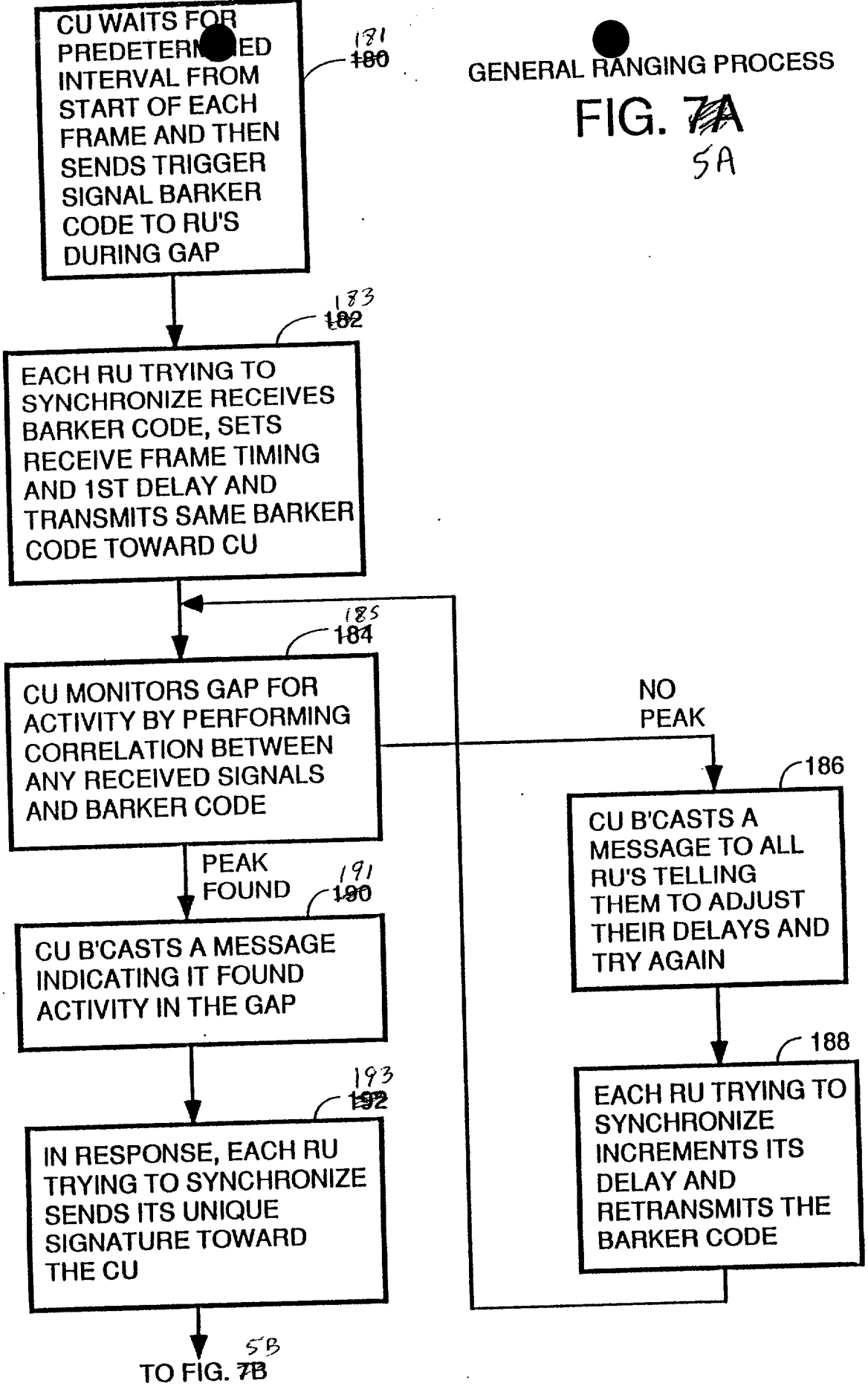

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
FRAME
#1
INTERVAL
= T_F
T_{CU}
T_{NEAR}
T_{FAR}
170
132
137
116
135
196
190
139
118
122
136
192
194
120
141
134
127
130
126
125
123
128
131
124
106
133

FIG. 4

GENERAL RANGING PROCESS

FIG. 7A

5A



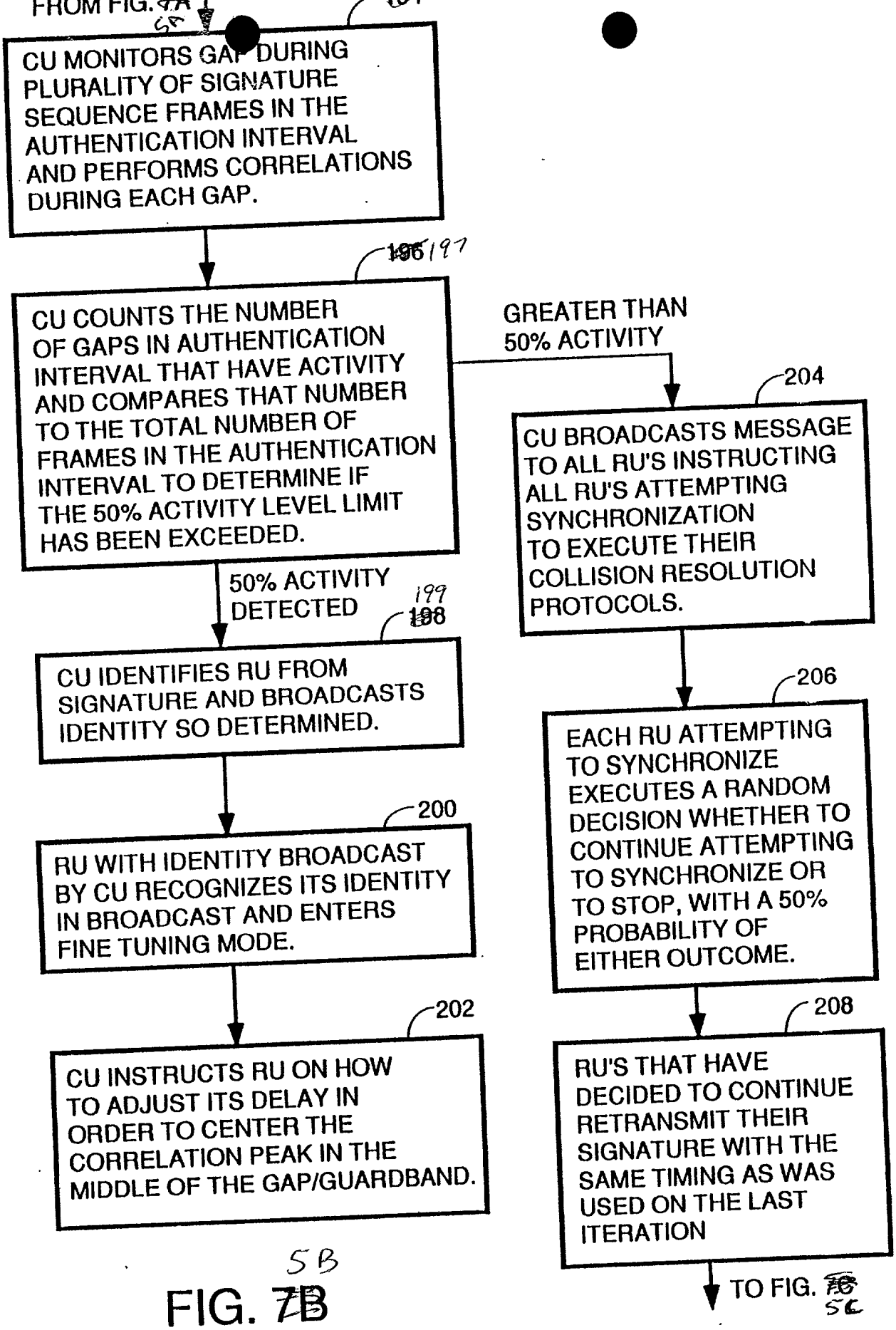

FROM FIG. 4A
5B
CU MONITORS GAP DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
196/197
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
GREATER THAN 50% ACTIVITY
204
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
50% ACTIVITY DETECTED
198/199
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
206
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
200
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
202
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.
208
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. 5C

FIG. 7B

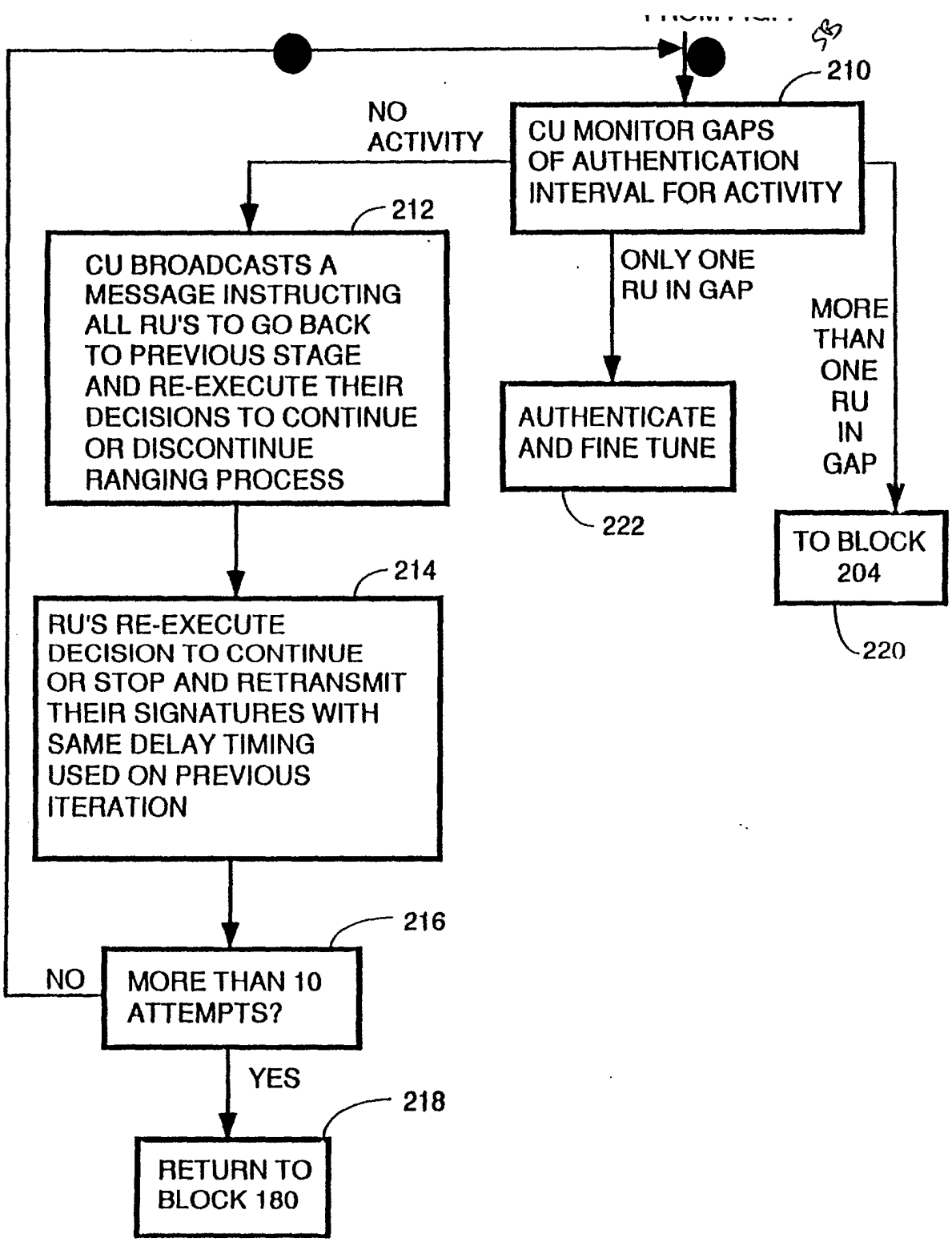
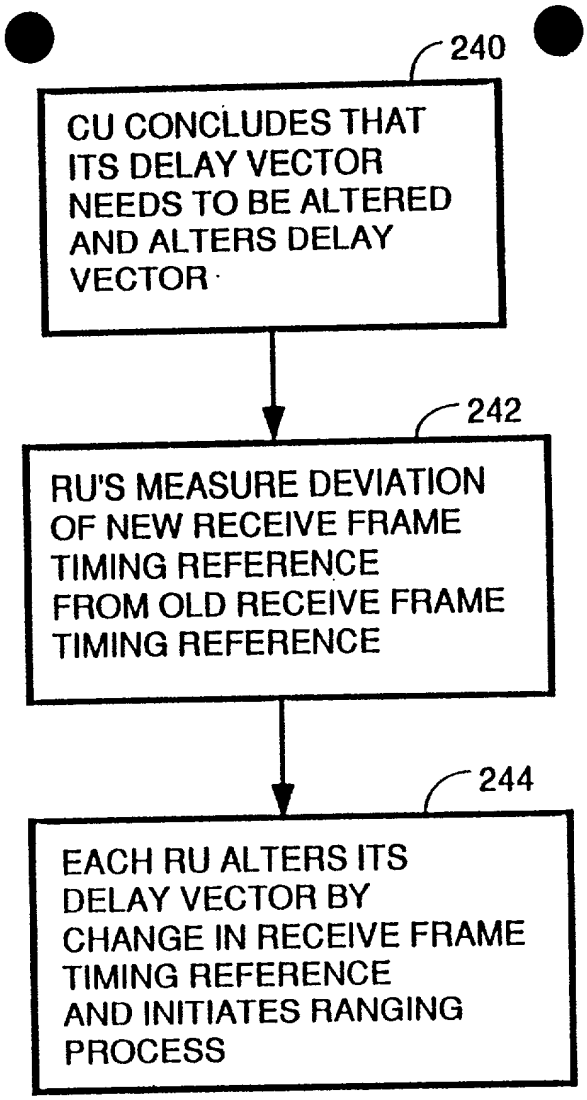

FROM FIG. 5
210
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
NO ACTIVITY
ONLY ONE RU IN GAP
MORE THAN ONE RU IN GAP
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
AUTHENTICATE AND FINE TUNE
222
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. 5C ~~7C~~



6

FIG. 8

DEAD RECKONING RE-SYNC

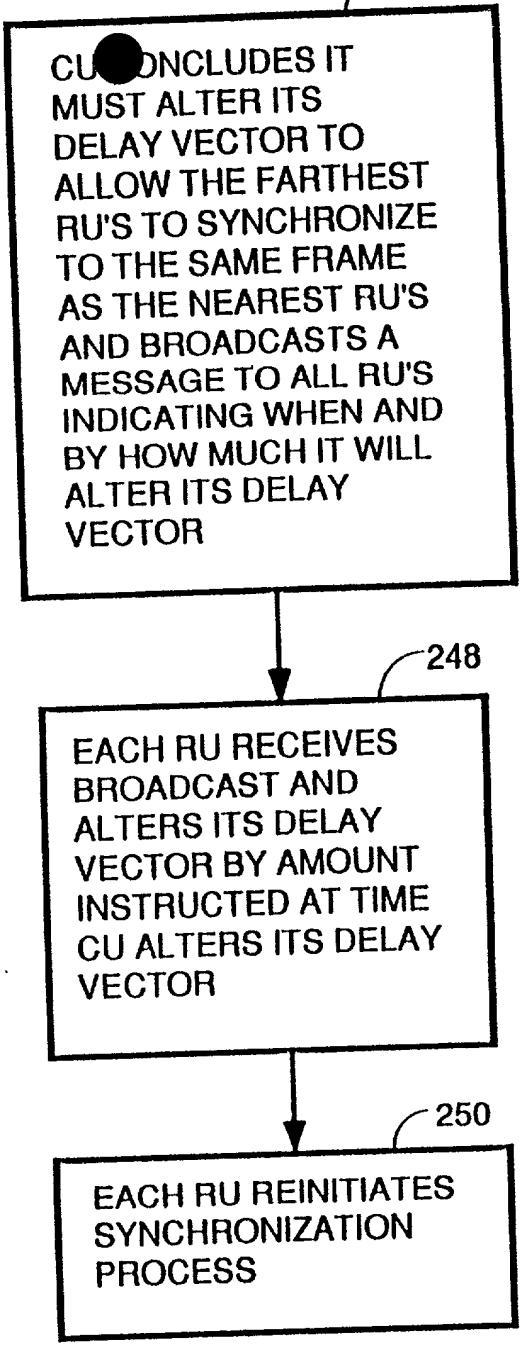
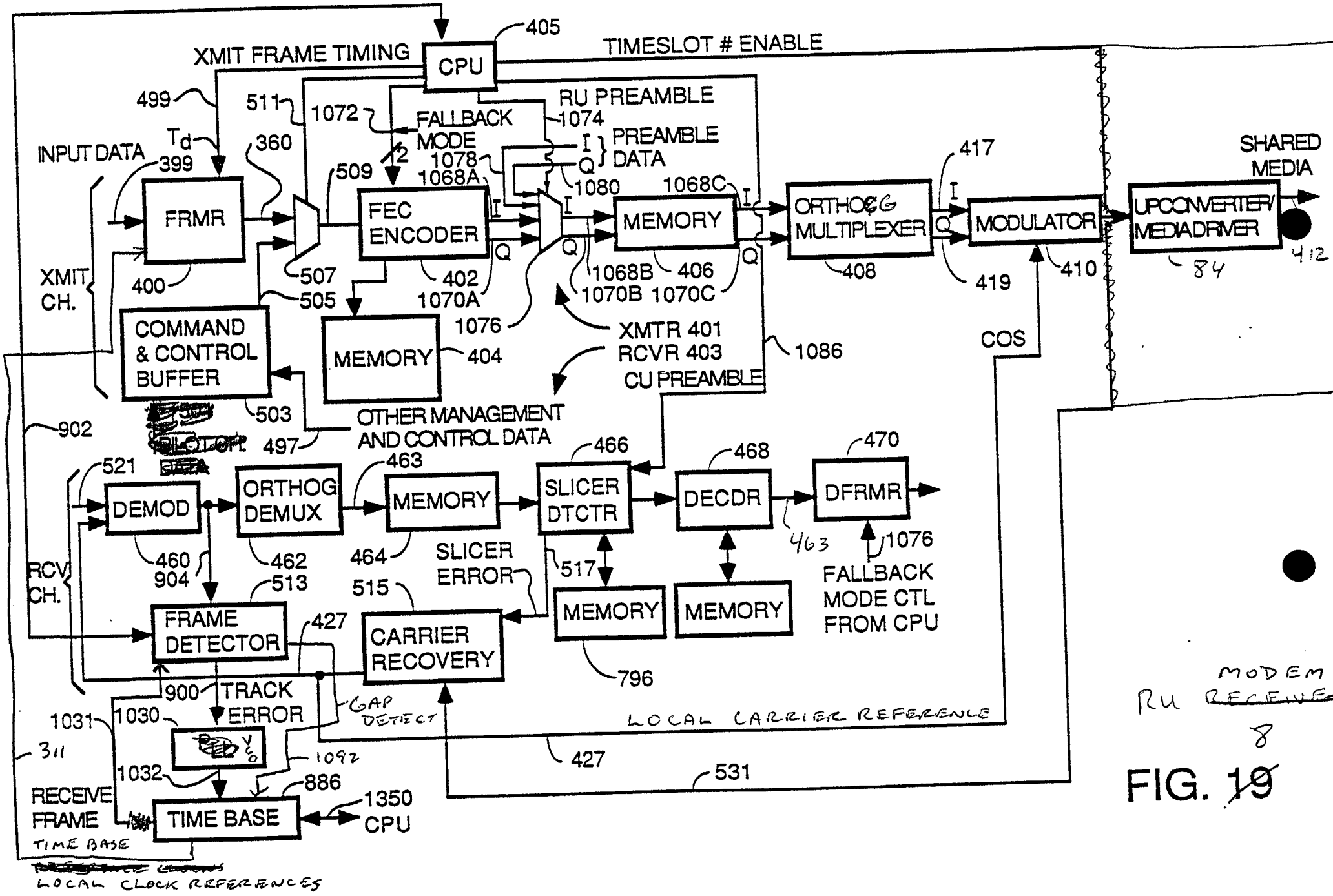


FIG. 9

PRECURSOR EMBODIMENT

RU

DIGITAL MODEM BLOCK DIAGRAM



MODEM RU RECEIVE

8

FIG. 19

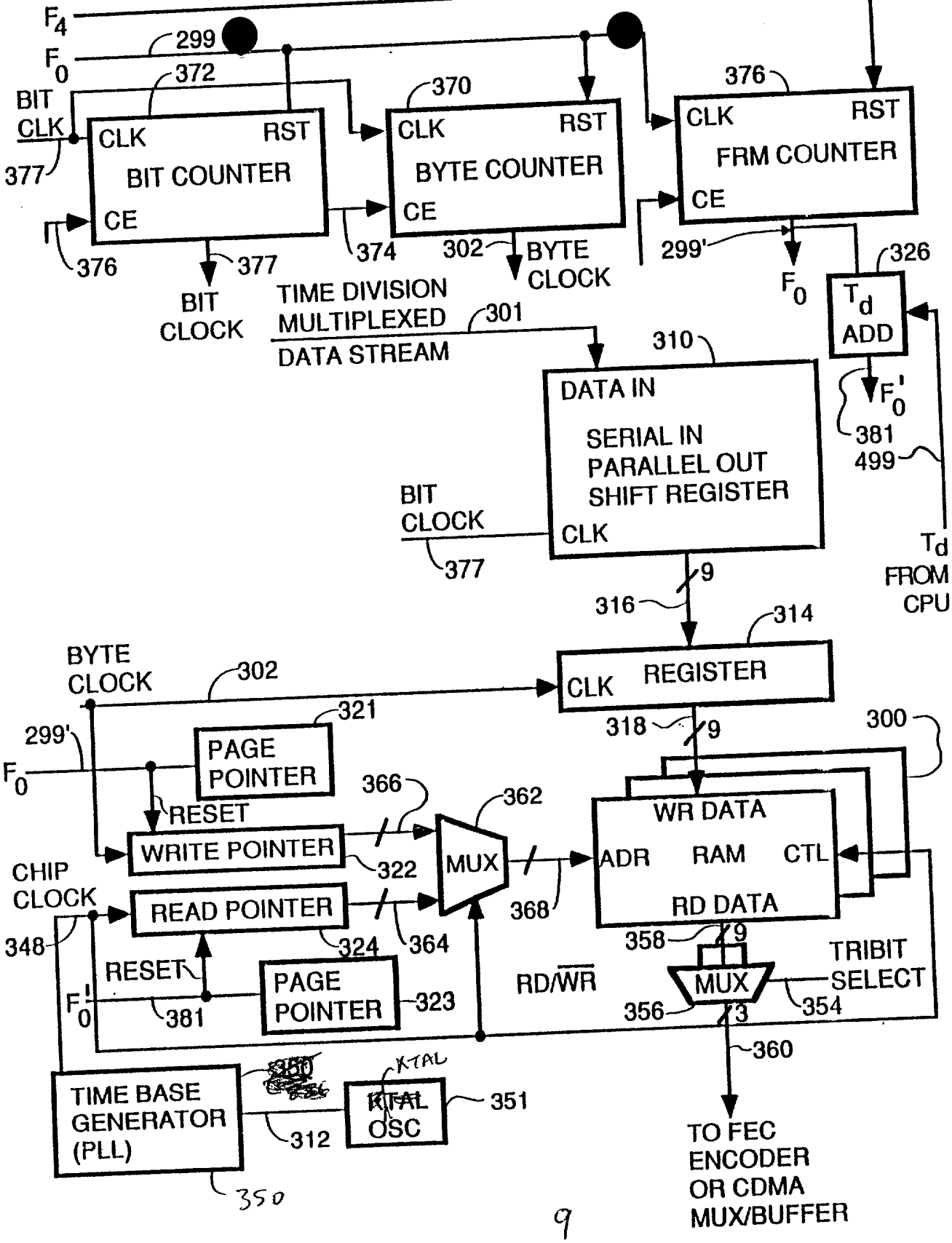

F4
F0
299
372
370
376
BIT CLK
CLK
RST
BIT COUNTER
CE
BYTE COUNTER
FRM COUNTER
377
376
374
302
BYTE CLOCK
299'
326
BIT CLOCK
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
Td ADD
F'0
381
499
Td FROM CPU
9
316
314
REGISTER
318
300
321
PAGE POINTER
RESET
366
362
WRITE POINTER
322
MUX
WR DATA
ADR
RAM
CTL
RD DATA
CHIP CLOCK
READ POINTER
324
364
368
348
358
TRIBIT SELECT
RD/WR
356
354
323
360
TIME BASE GENERATOR (PLL)
XTAL
OSC
351
312
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. 12

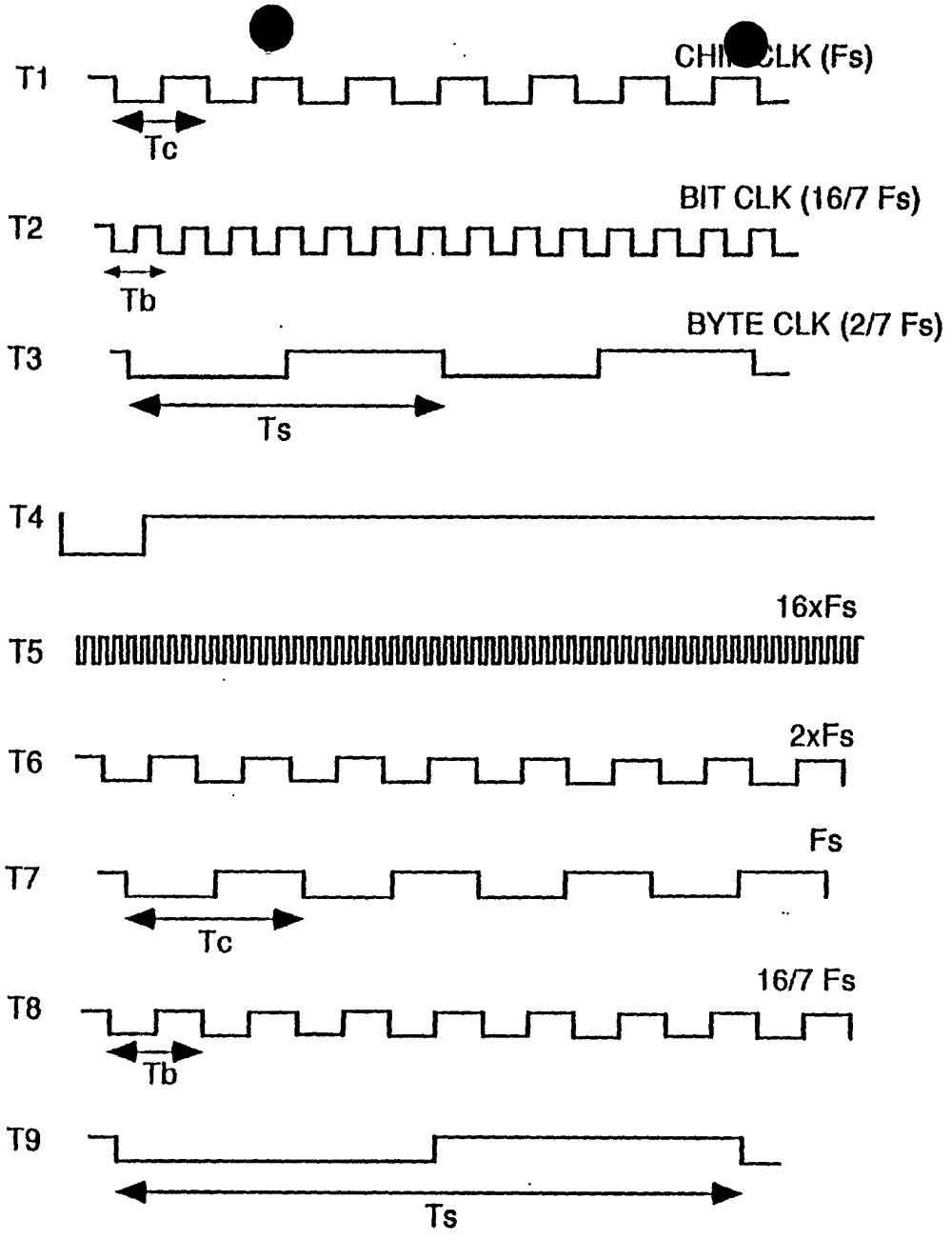
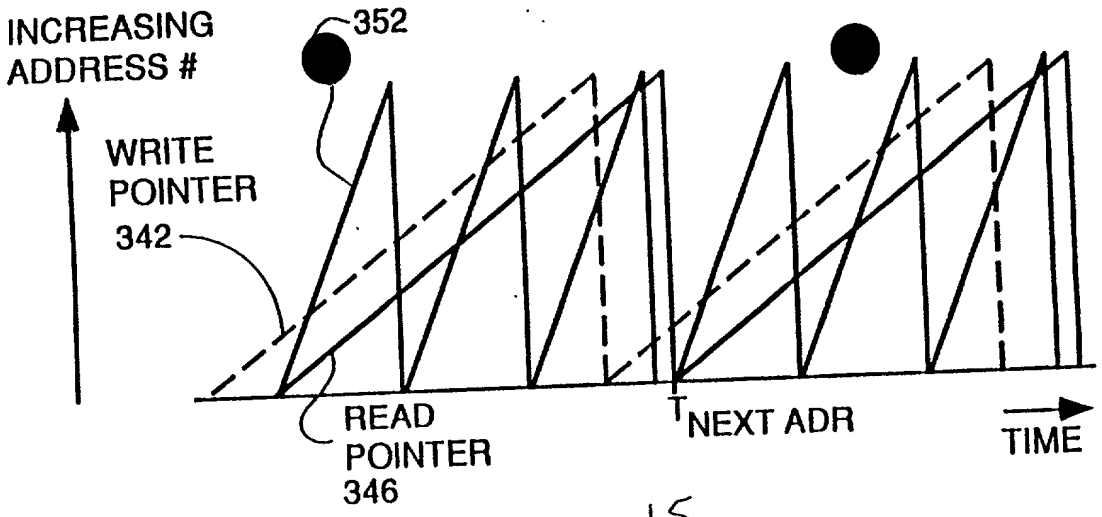
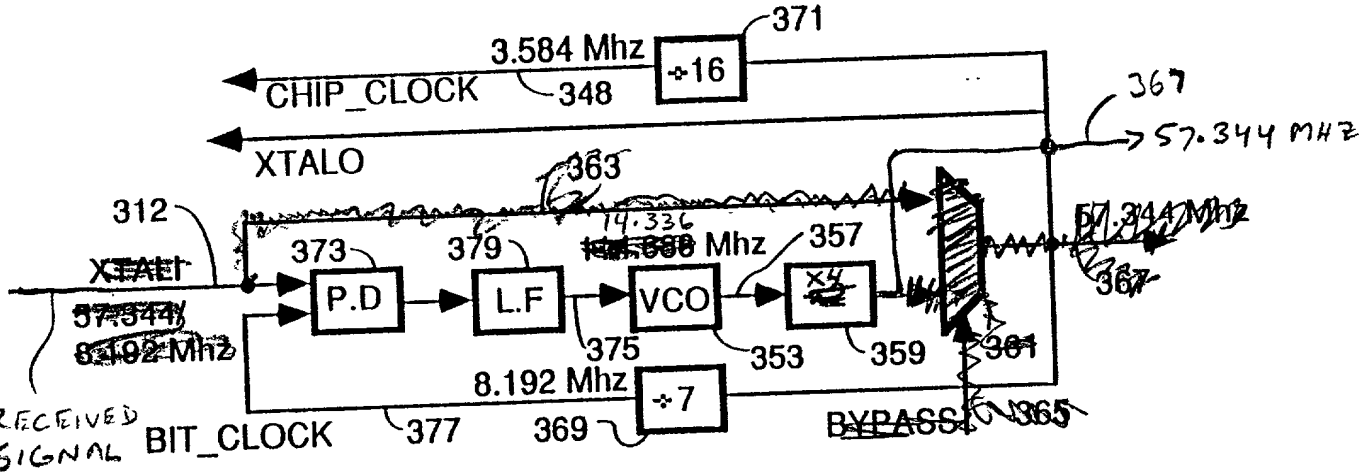

T1
CHI CLK (Fs)
Tc
T2
BIT CLK (16/7 Fs)
Tb
T3
BYTE CLK (2/7 Fs)
Ts
T4
T5
16xFs
T6
2xFs
T7
Fs
Tc
T8
16/7 Fs
Tb
T9
Ts

FIG. 13



15

FIG. 17



11

FIG. 18

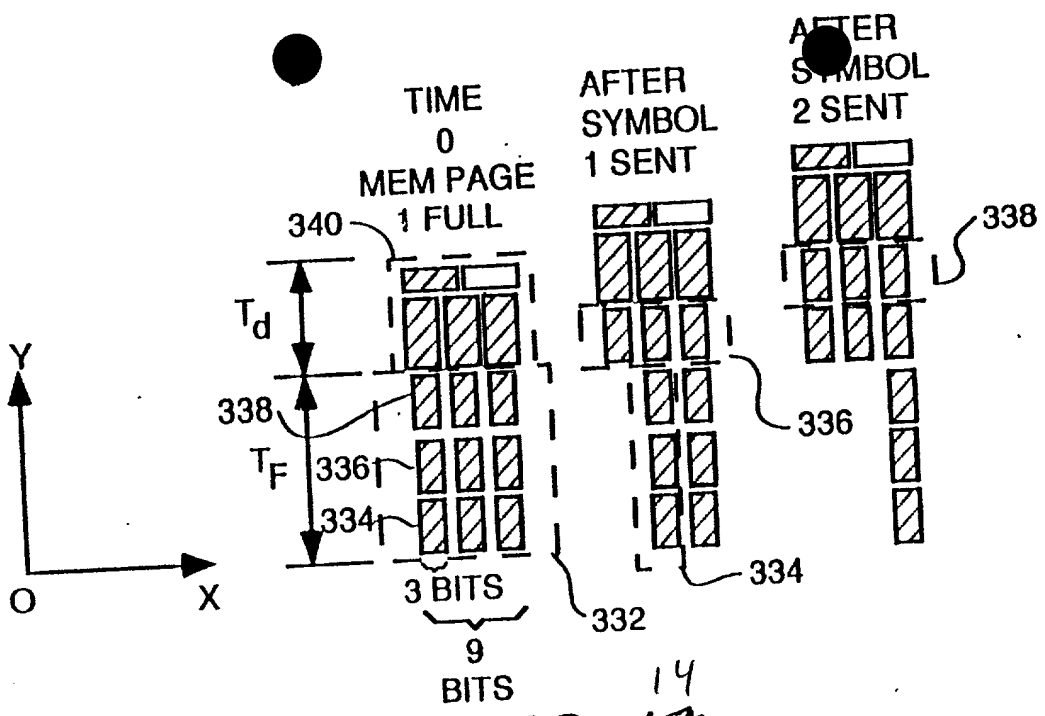


FIG. 14

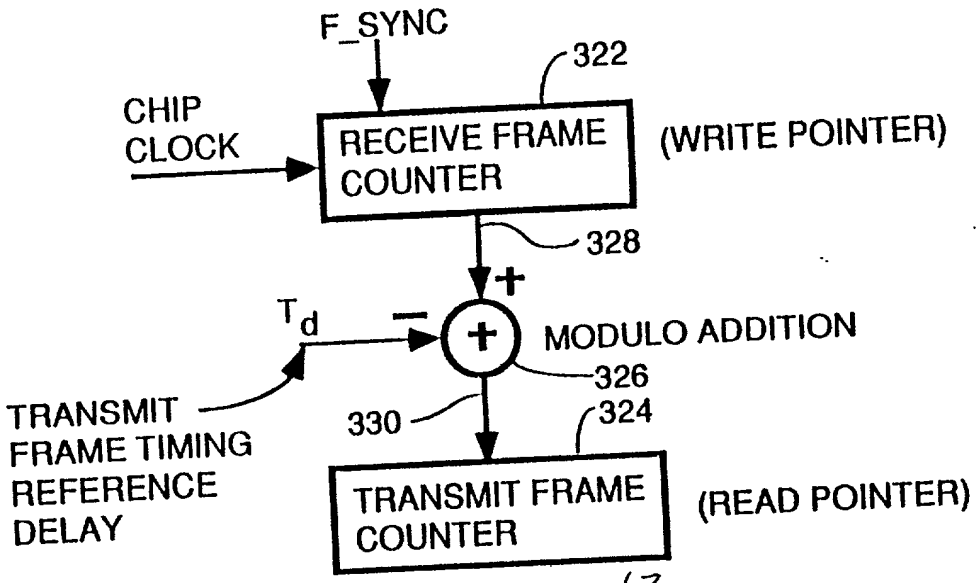


FIG. 12

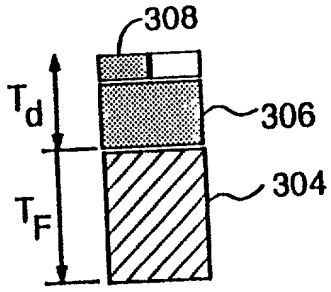


FIG. 13

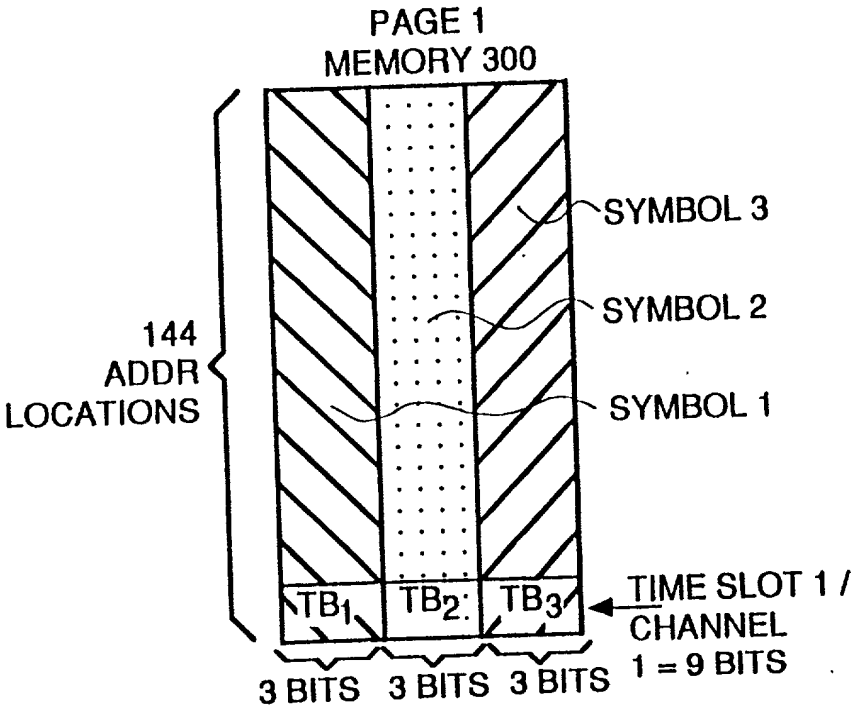
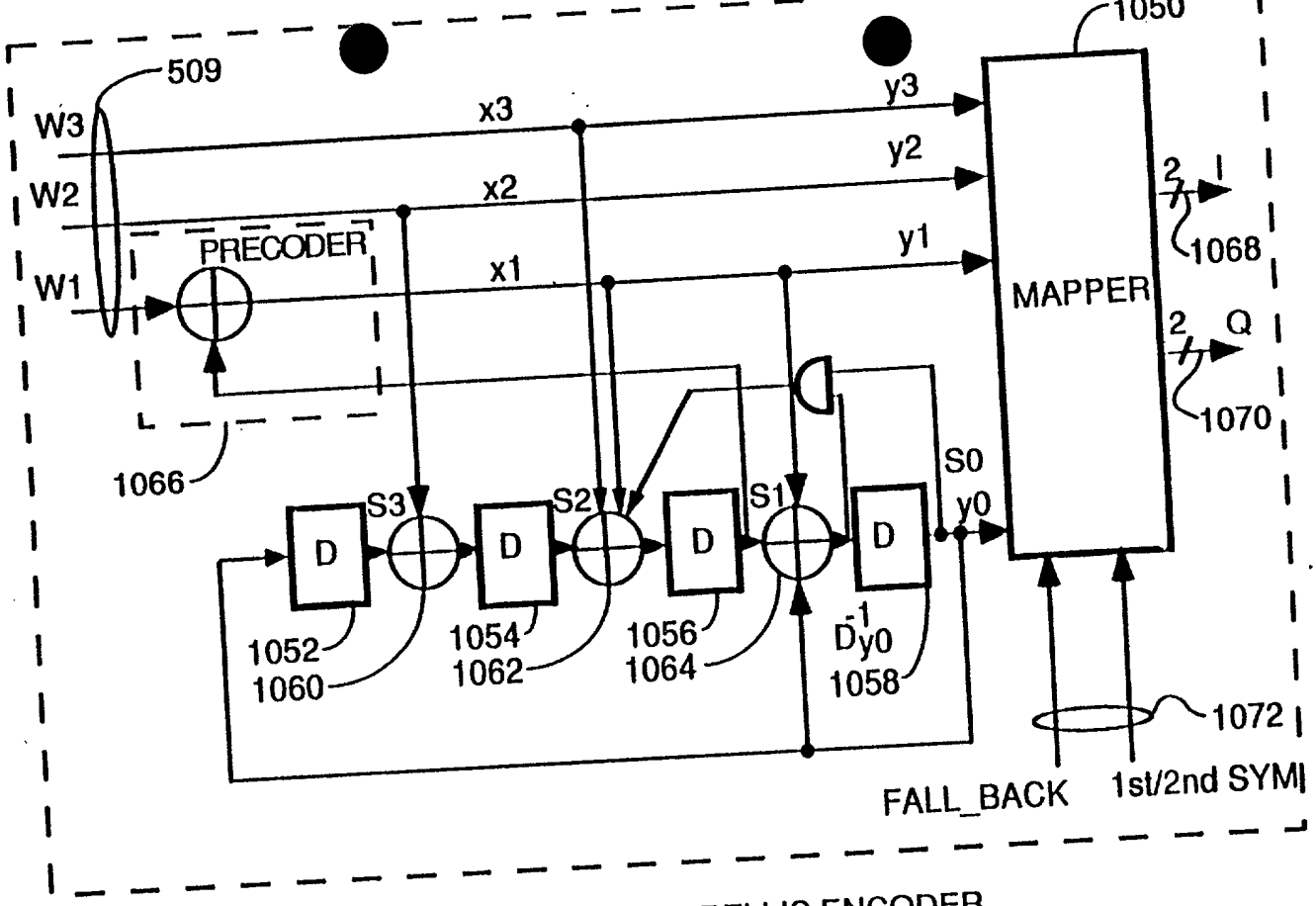

PAGE 1
MEMORY 300
SYMBOL 3
SYMBOL 2
SYMBOL 1
144
ADDR
LOCATIONS
TB1
TB2
TB3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS
3 BITS
3 BITS

FIG. 20

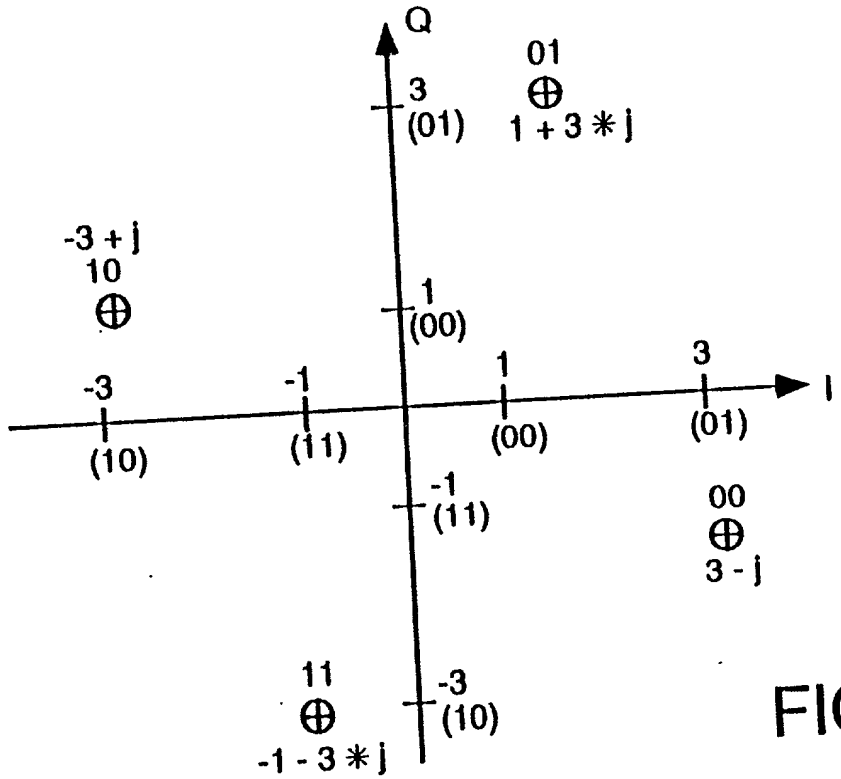


PREFERRED TRELLIS ENCODER

FIG. 42

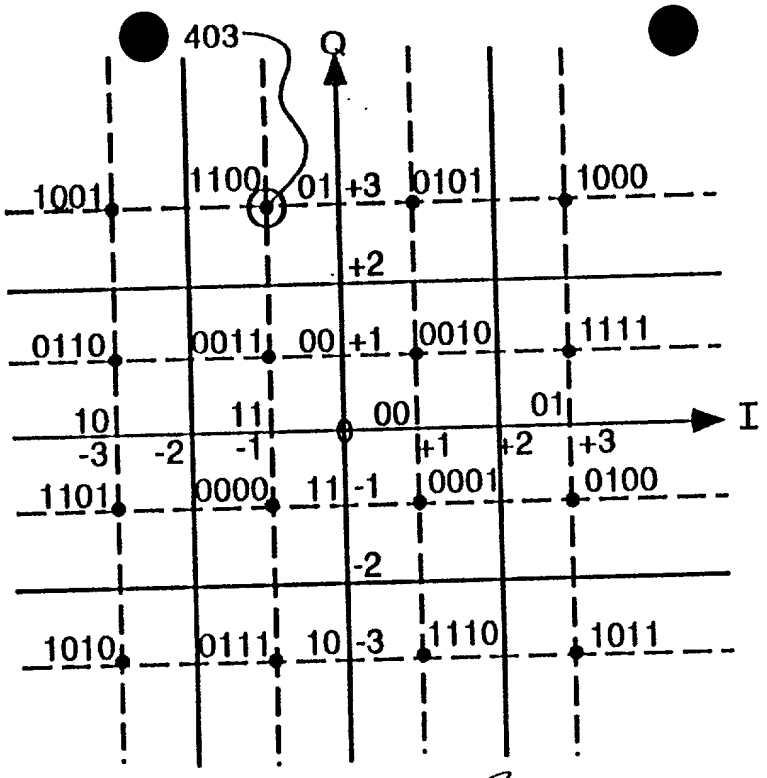
17

MAPPING FOR FALL-BACK MODE - LSB'S



21

FIG. 43



18

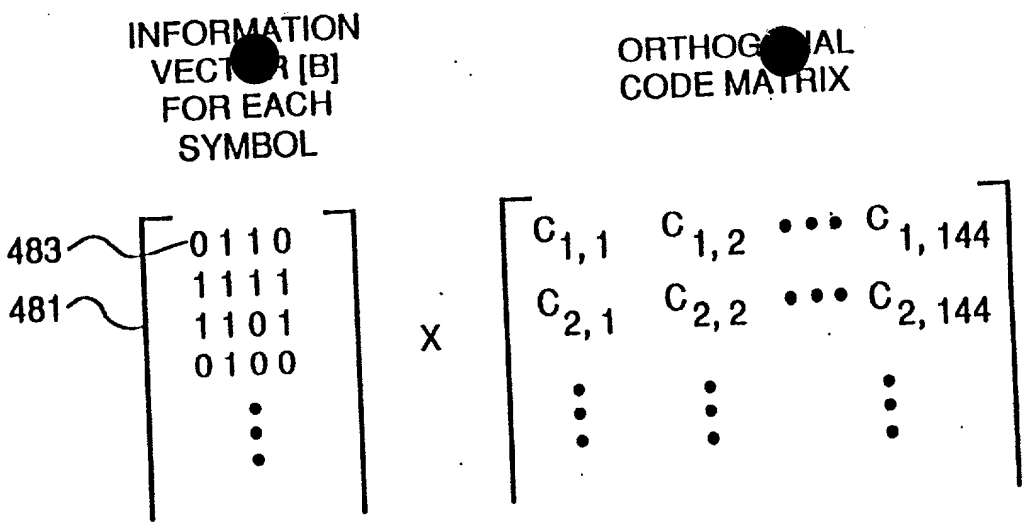
FIG. 21

CODE	INPHASE	QUADRATURE	
0000	111	111	= -1 - j
0001	001	111	= 1 - j
0010	001	001	= 1+ j
0011	111	001	= -1+ j
0100	011	111	= 3 - j
0101	001	011	= 1+ 3* j
0110	101	001	= -3 + j
0111	111	101	= -1 - 3* j
1000	011	011	=+3 + 3*j
1001	101	011	= -3 + 3*j
1010	101	101	= -3 - 3* j
1011	011	101	= 3 - 3* j
1100	111	011	= -1+ 3* j
1101	101	111	= -3 - j
1110	001	101	= 1 - 3* j
1111	011	001	= 3 + j

403

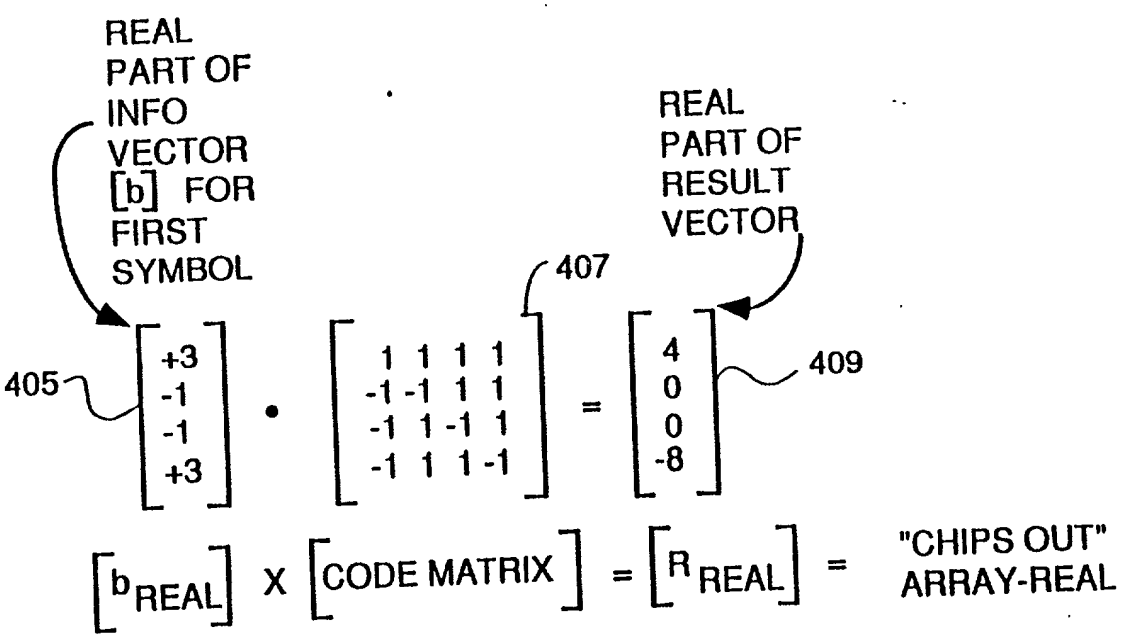
19

FIG. 22



20A

FIG. ~~23~~A



20B

FIG. ~~23~~B

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. ~~44~~ 22

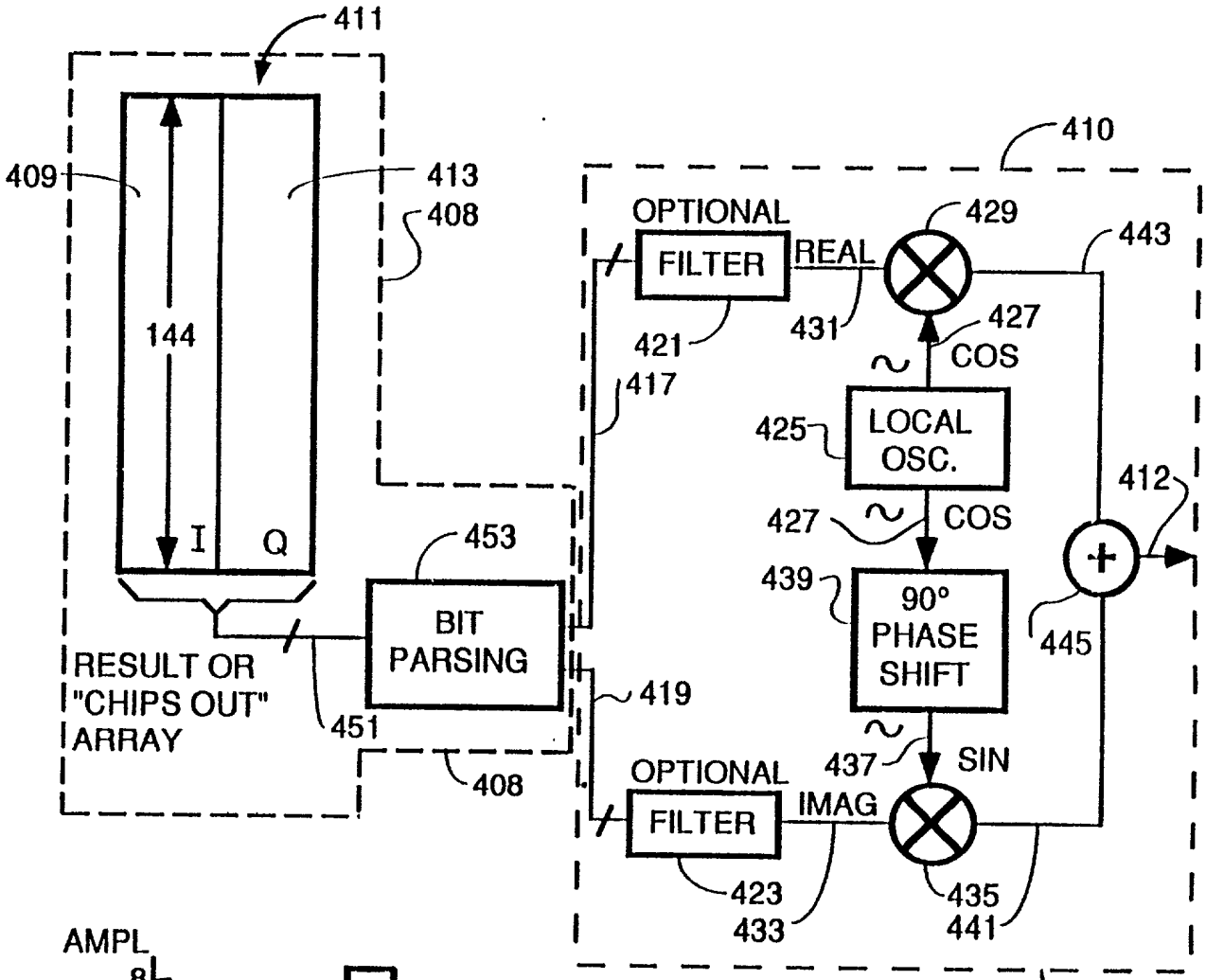

411
409
413
408
144
I
Q
453
BIT PARSING
RESULT OR "CHIPS OUT" ARRAY
451
408
410
OPTIONAL
FILTER
REAL
421
431
429
443
427
COS
417
425
LOCAL OSC.
427
COS
412
439
90° PHASE SHIFT
445
419
437
SIN
OPTIONAL
FILTER
IMAG
423
433
435
441
410

FIG. 24

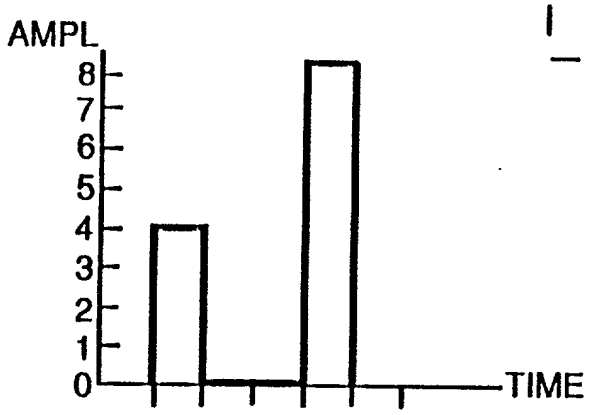
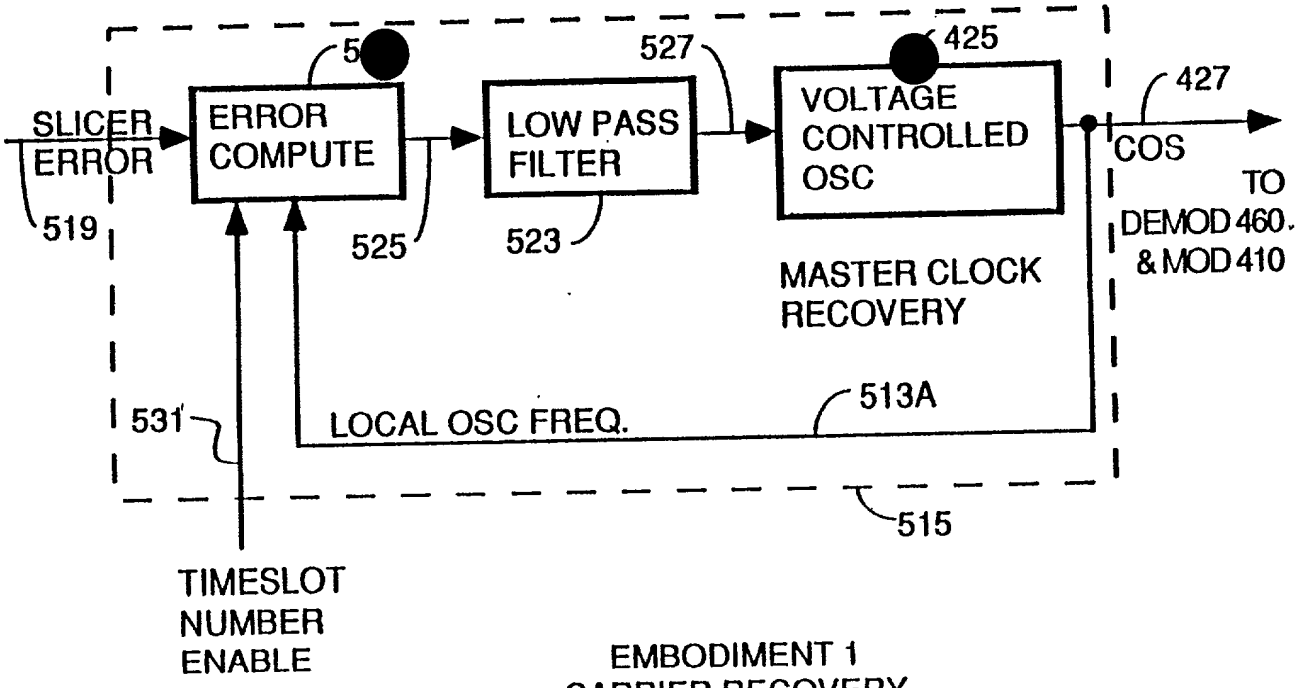

AMPL
8
7
6
5
4
3
2
1
0
TIME

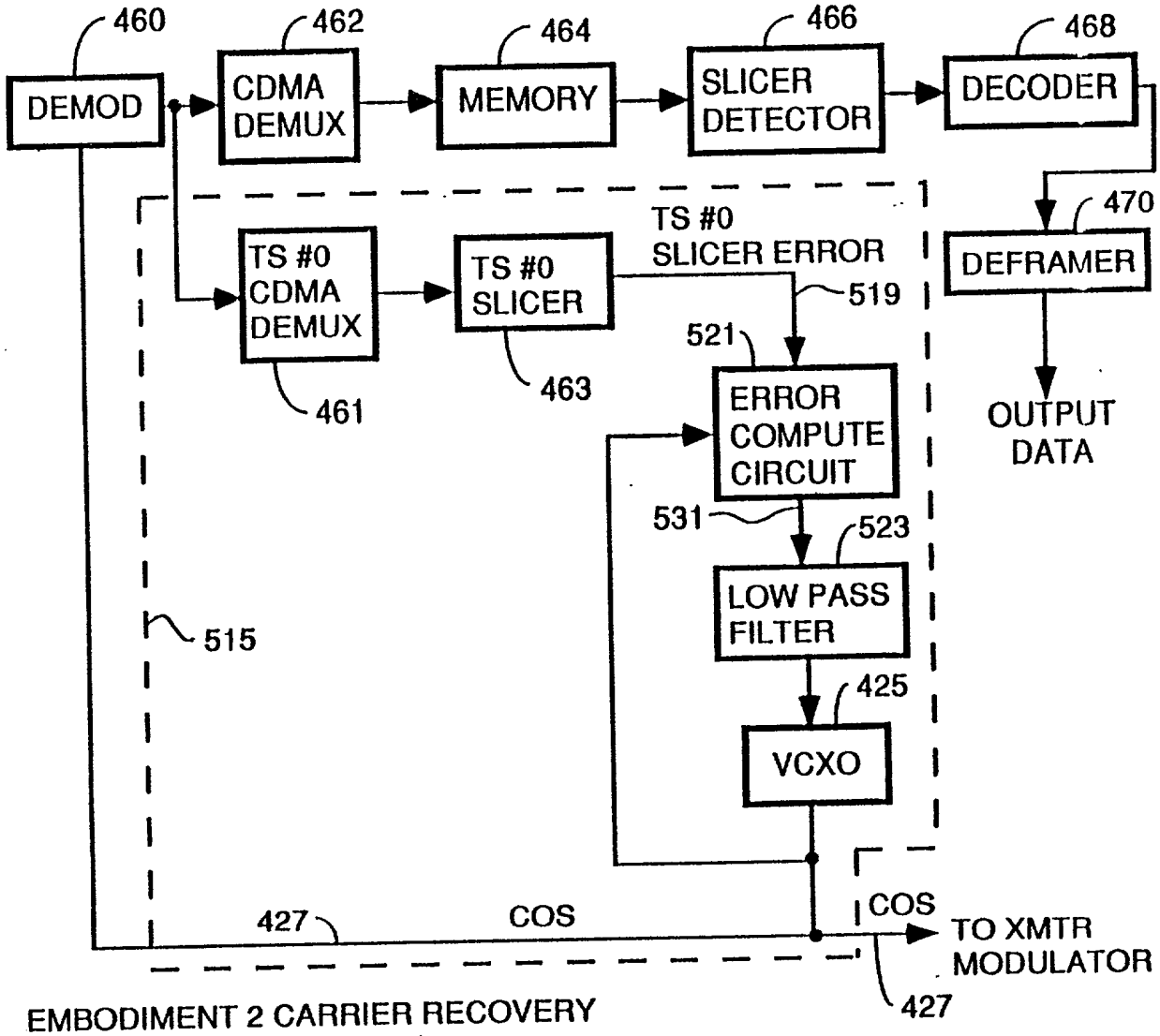
FIG. 25



EMBODIMENT 1
CARRIER RECOVERY

FIG. 35

25



EMBODIMENT 2 CARRIER RECOVERY

FIG. 36

26

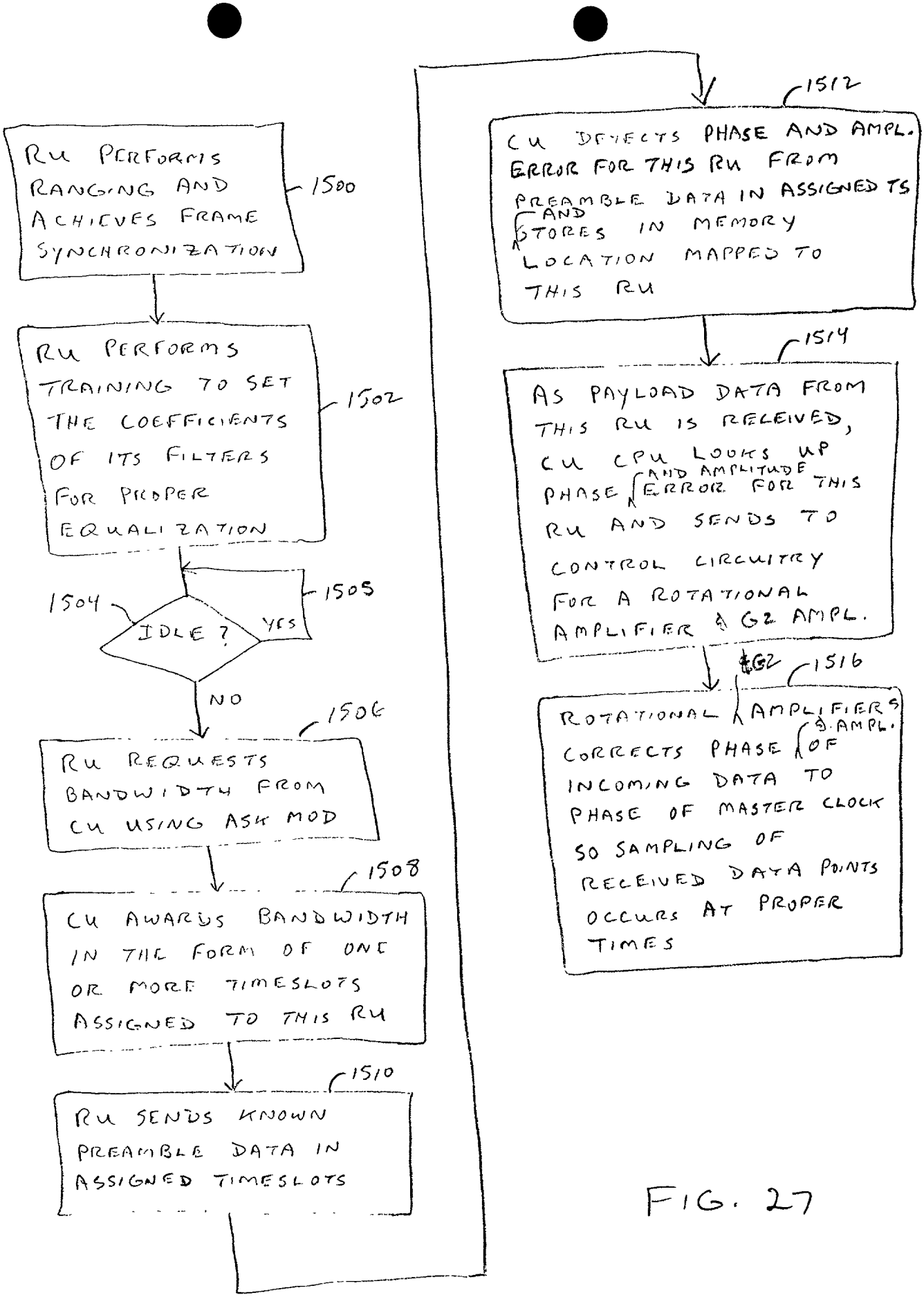
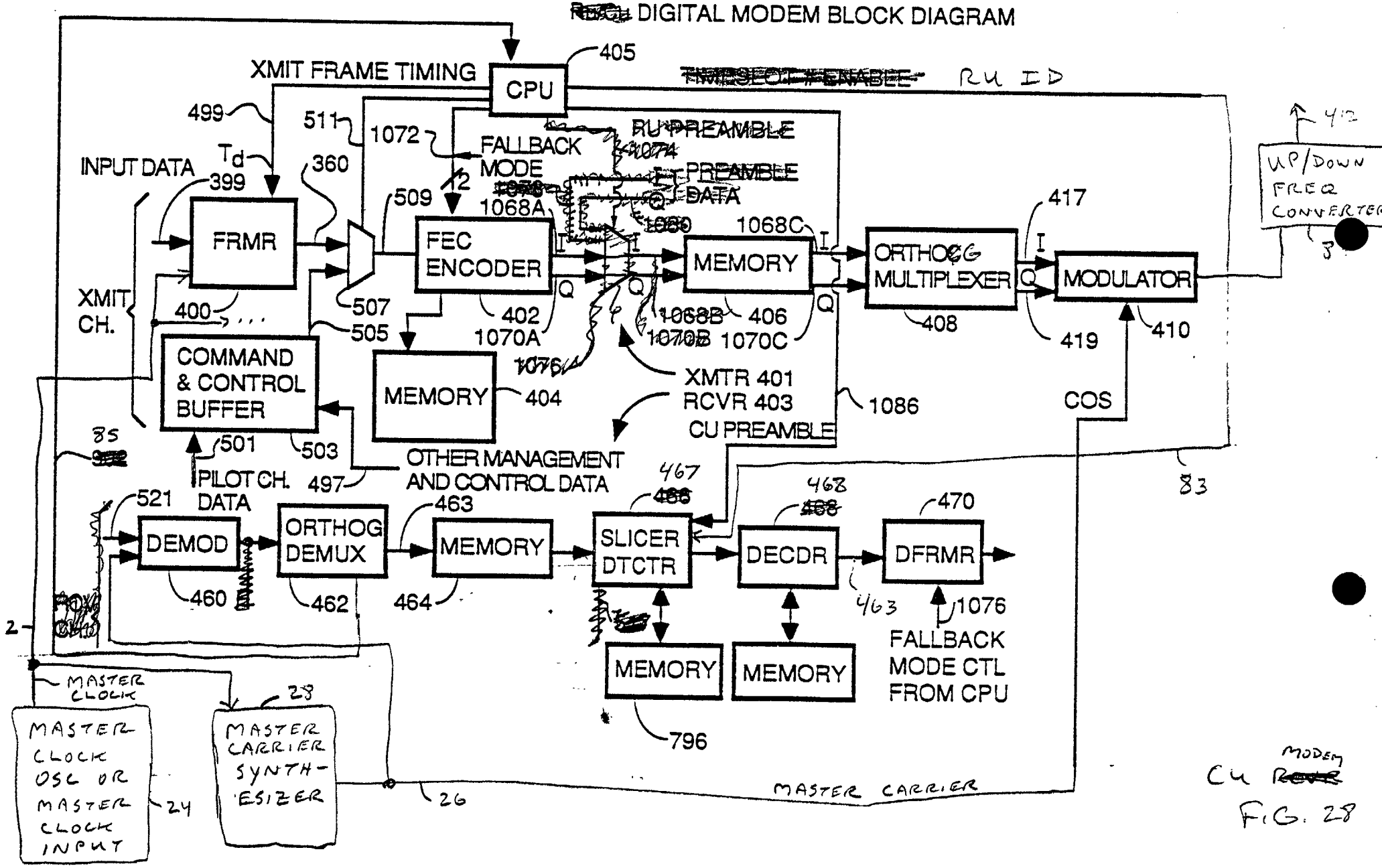

RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1500
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1502
1504
IDLE ?
YES
1505
NO
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1506
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1508
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1510
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED TS AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1512
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1514
ROTATIONAL AMPLIFIER & G2 AMPL. CORRECTS PHASE OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES
1516

FIG. 27

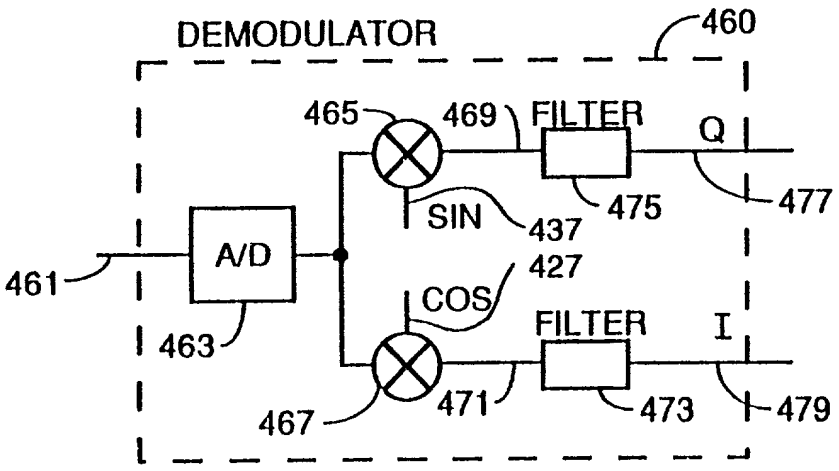
CU

DIGITAL MODEM BLOCK DIAGRAM



MODEM CU

FIG. 28



29

FIG. 26

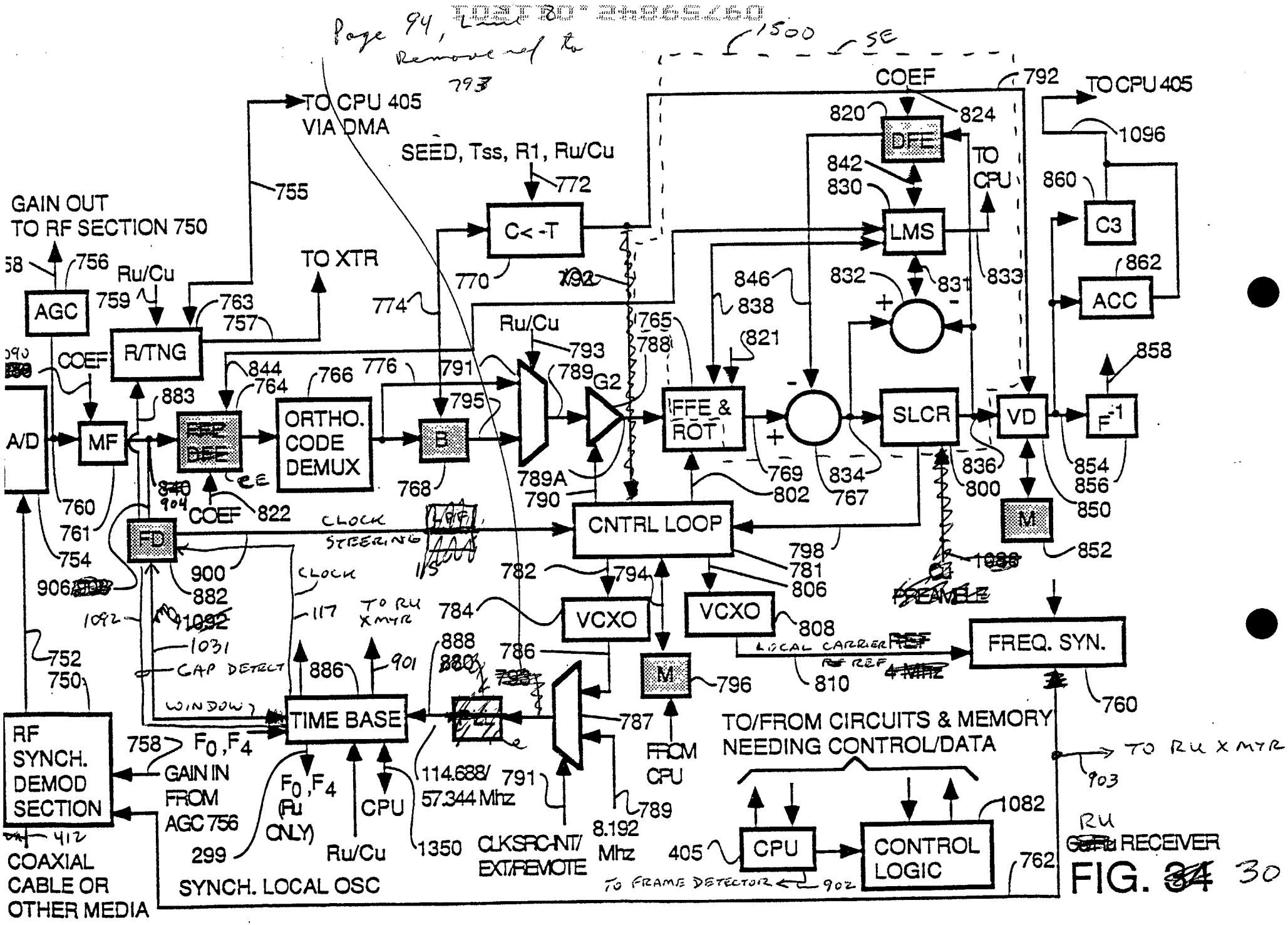

TO CPU 405 VIA DMA
SEED, Tss, R1, Ru/Cu
772
755
GAIN OUT TO RF SECTION 750
AGC
759
Ru/Cu
R/TNG
763
757
TO XTR
C<-T
770
774
Ru/Cu
793
COEF
844
764
766
776
791
789
G2
795
883
ORTHO. CODE DEMUX
B
768
789A
790
765
788
821
838
846
832
831
833
LMS
DFE
820
824
842
830
TO CPU
792
TO CPU 405
1096
860
C3
862
ACC
858
F-1
854
856
850
VD
836
800
SLCR
IFFE & ROT
769
802
834
767
M
852
A/D
MF
FFE DFE
COEF
822
760
761
754
906
904
FD
CLOCK STEERING
CNTRL LOOP
798
781
806
782
794
900
882
CLOCK
117
TO RU XMTR
784
VCXO
VCXO
808
1092
1031
CAP DETECT
WINDOW
752
750
886
901
888
786
787
M
796
FREQ. SYN.
760
LOCAL CARRIER REF
RF REF 4 MHz
810
TIME BASE
TO/FROM CIRCUITS & MEMORY NEEDING CONTROL/DATA
FROM CPU
758
F0, F4
GAIN IN FROM AGC 756
F0, F4 (Ru ONLY)
CPU
Ru/Cu
114.688/ 57.344 Mhz
791
8.192 Mhz
789
CLKSRC-NT/ EXT/REMOTE
1350
299
405
CPU
CONTROL LOGIC
1082
762
TO FRAME DETECTOR
902
903
TO RU XMTR
RU RECEIVER
RF SYNCH. DEMOD SECTION
412
COAXIAL CABLE OR OTHER MEDIA
SYNCH. LOCAL OSC

FIG. 30

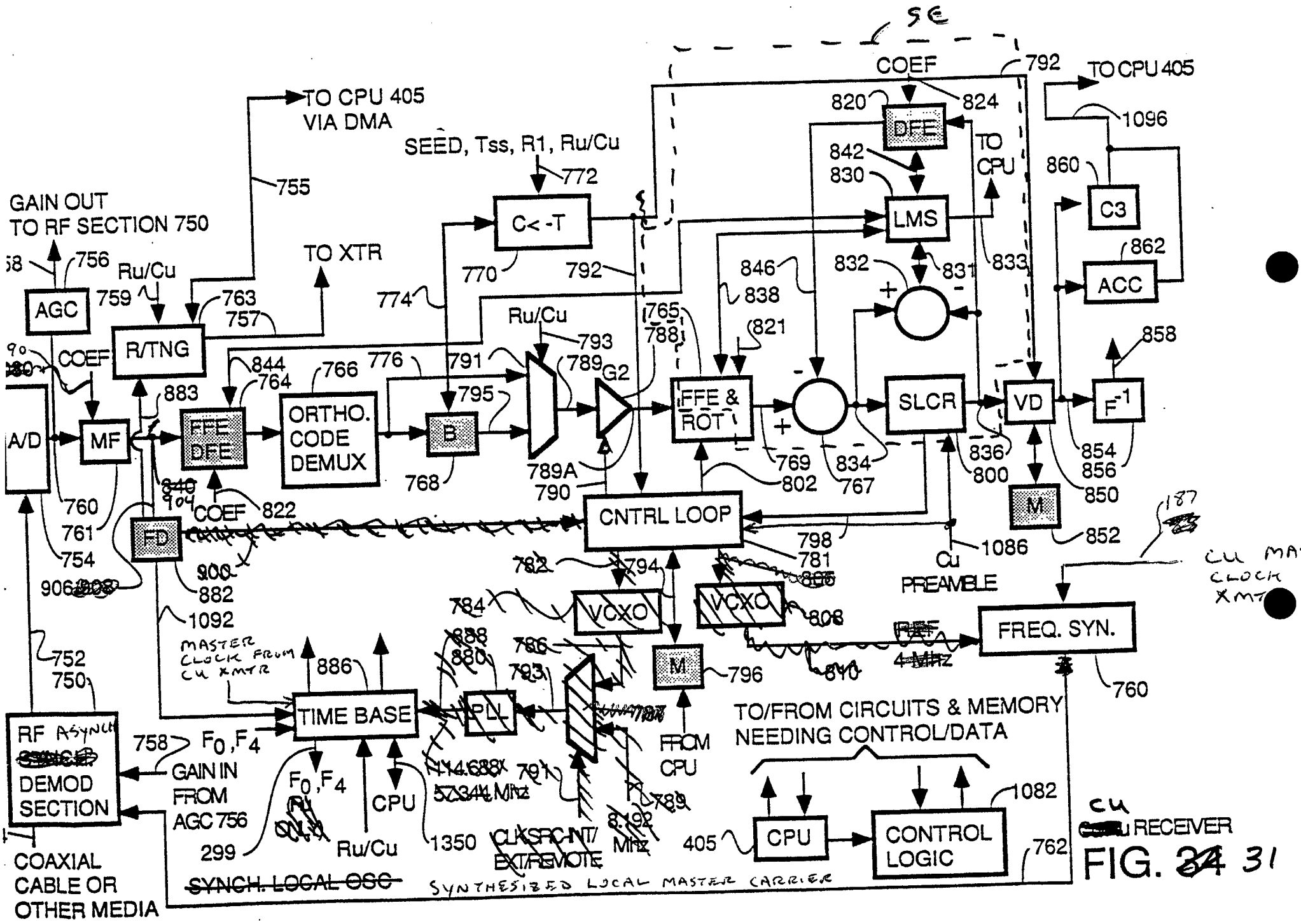

5E
TO CPU 405
VIA DMA
SEED, Tss, R1, Ru/Cu
772
755
GAIN OUT
TO RF SECTION 750
TO XTR
AGC
759
756
Ru/Cu
763
757
R/TNG
COEF
844
764
883
766
776
791
793
789
G2
795
ORTHO.
CODE
DEMUX
B
768
789A
790
774
770
C<-T
792
Ru/Cu
765
788
821
838
846
832
831
833
LMS
DFE
842
830
820
824
COEF
792
TO CPU 405
1096
TO
CPU
860
C3
862
ACC
858
F-1
854
856
850
VD
836
800
SLCR
FFE &
ROT
769
834
767
802
M
852
A/D
MF
FFE
DFE
760
761
754
906
908
840
904
COEF
822
FD
900
882
1092
CNTRL LOOP
798
781
782
794
1086
Cu
PREAMBLE
187
CU MAST
CLOCK F
XMT
784
VCXO
VCXO
808
786
888
880
793
M
796
840
FREQ. SYN.
4 MHz
760
752
750
MASTER
CLOCK FROM
CU XMTR
886
TIME BASE
PLL
TO/FROM CIRCUITS & MEMORY
NEEDING CONTROL/DATA
FROM
CPU
RF ASYNCH
DEMOD
SECTION
758
F_0, F_4
GAIN IN
FROM
AGC 756
F_0, F_4
CPU
Ru/Cu
1350
CLK SRC INT/
EXT/REMOTE
8.192
MHz
789
405
CPU
CONTROL
LOGIC
1082
762
299
SYNCH. LOCAL OSC
SYNTHESIZED LOCAL MASTER CARRIER
COAXIAL
CABLE OR
OTHER MEDIA
CU
RECEIVER

FIG. 34 31

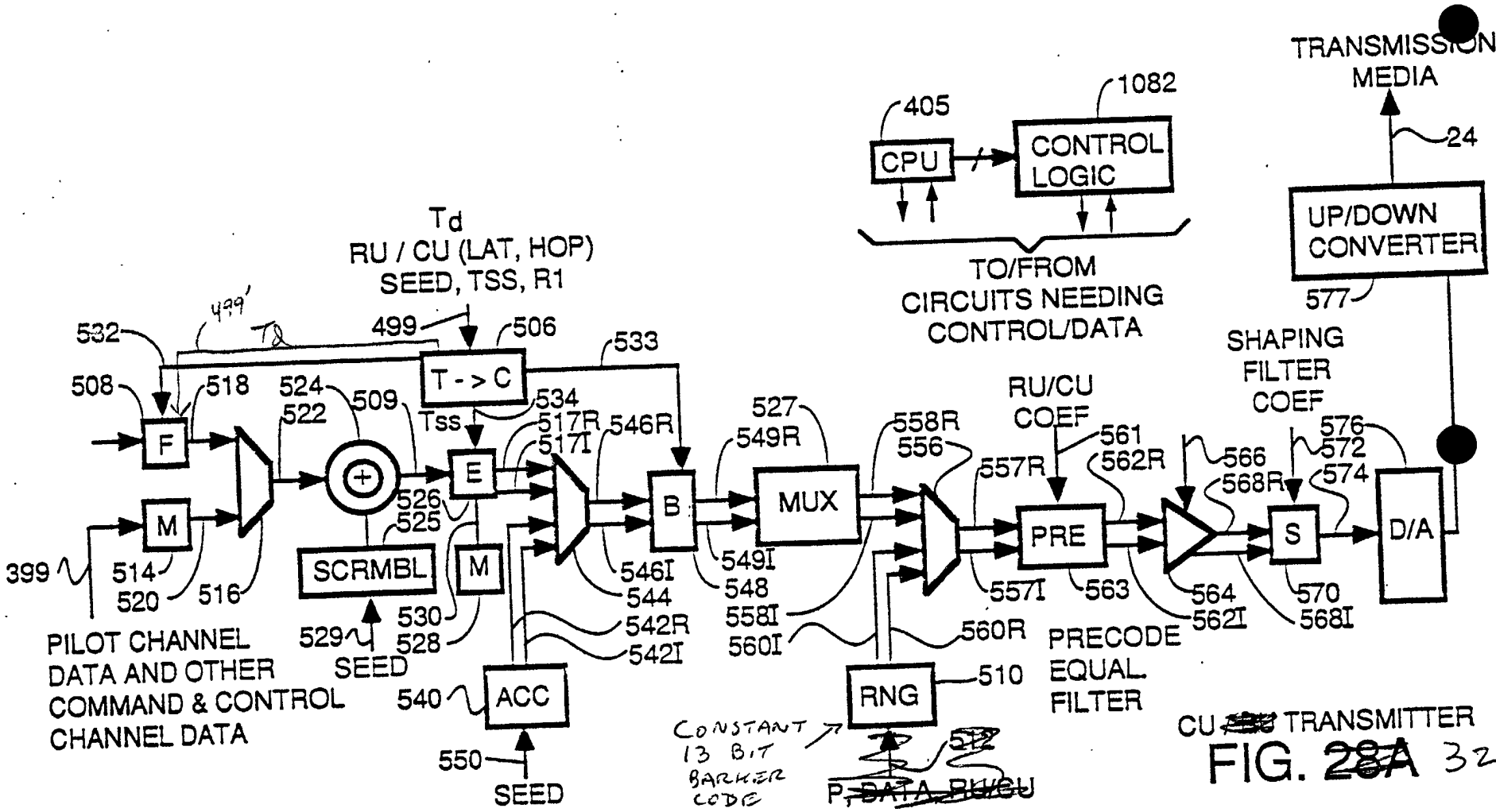

TRANSMISSION MEDIA
24
1082
405
CPU
CONTROL LOGIC
UP/DOWN CONVERTER
577
TO/FROM CIRCUITS NEEDING CONTROL/DATA
Td
RU / CU (LAT, HOP) SEED, TSS, R1
499'
Td
499
506
T -> C
533
532
508
518
524
522
509
534
Tss
517R
517I
546R
527
549R
558R
556
RU/CU COEF
561
562R
557R
SHAPING FILTER COEF
576
572
566
568R
574
F
M
399
514
520
516
526
525
SCRMBL
M
529
SEED
530
528
E
B
MUX
PRE
S
D/A
546I
544
542R
542I
549I
548
558I
560I
560R
557I
563
564
562I
570
568I
PILOT CHANNEL DATA AND OTHER COMMAND & CONTROL CHANNEL DATA
PRECODE EQUAL FILTER
540
ACC
550
SEED
CONSTANT 13 BIT BARKER CODE
RNG
510
P_DATA_RU/CU
CU TRANSMITTER

FIG. 28A 32

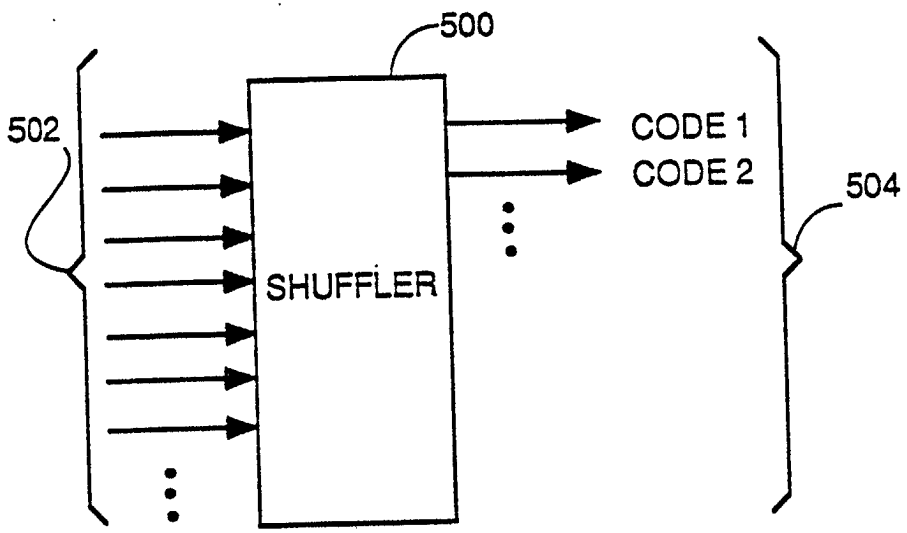


FIG. 27 38

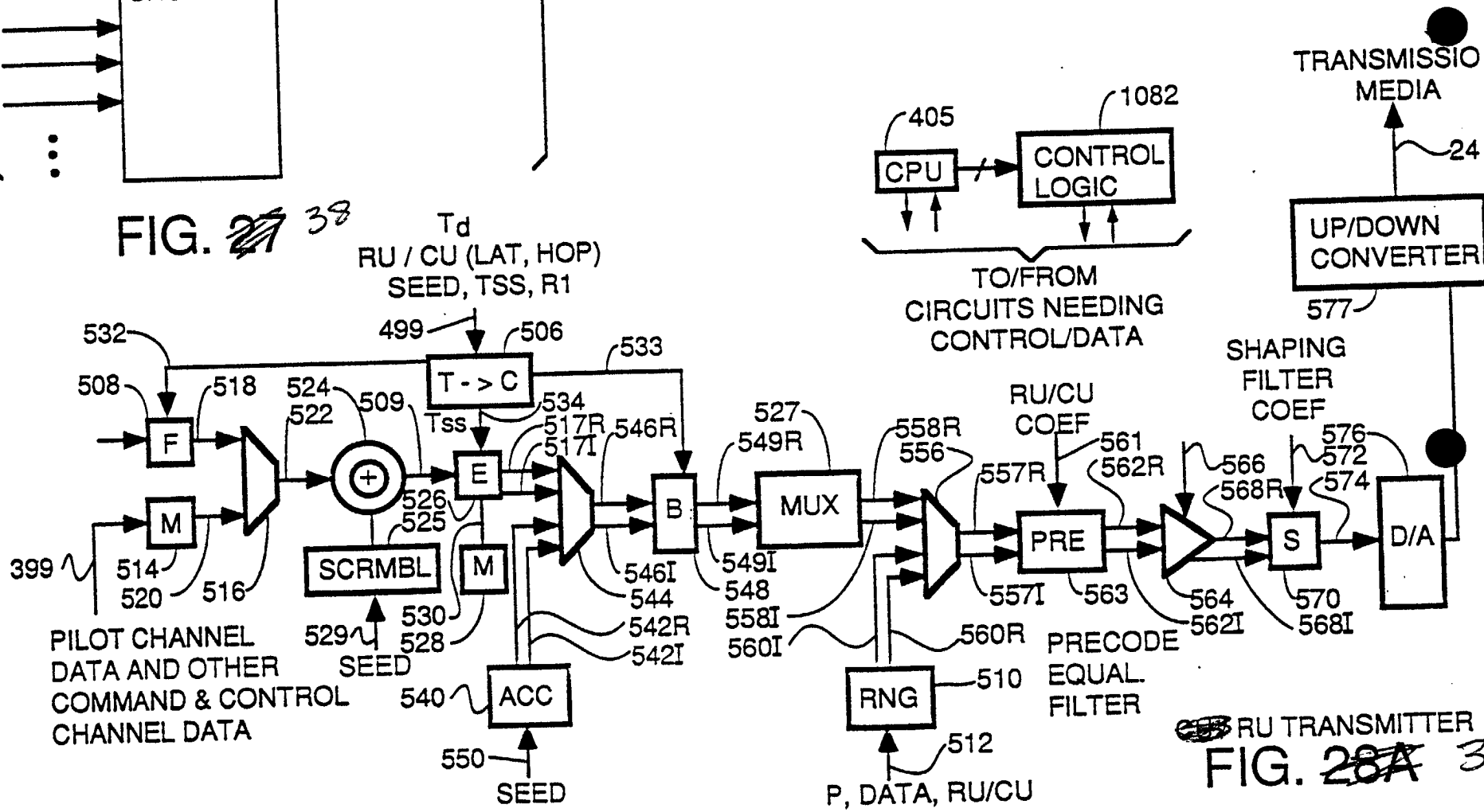


FIG. 28A 3

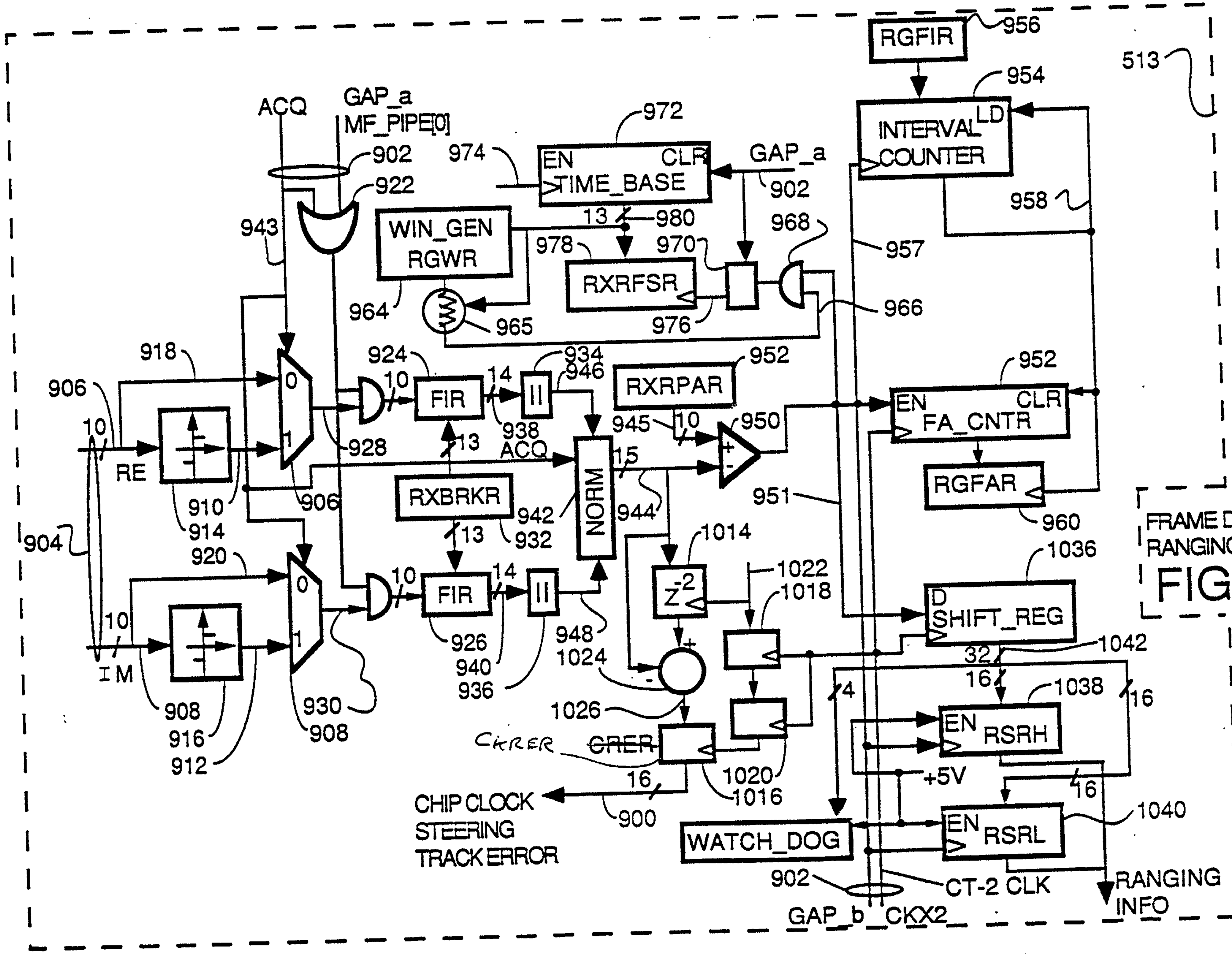

FRAME DETECTOR/
RANGING DETECTO
RGFIR
INTERVAL COUNTER
LD
EN
CLR
TIME_BASE
GAP_a
ACQ
GAP_a
MF_PIPE[0]
WIN_GEN
RGWR
RXRFSR
RXRPAR
FA_CNTR
RGFAR
FIR
NORM
RXBRKR
D
SHIFT_REG
RSRH
RSRL
+5V
WATCH_DOG
RANGING
INFO
CT-2 CLK
GAP_b
CKX2
RE
IM
CHIP CLOCK
STEERING
TRACK ERROR
GRER
Ckrer

FIG. 38

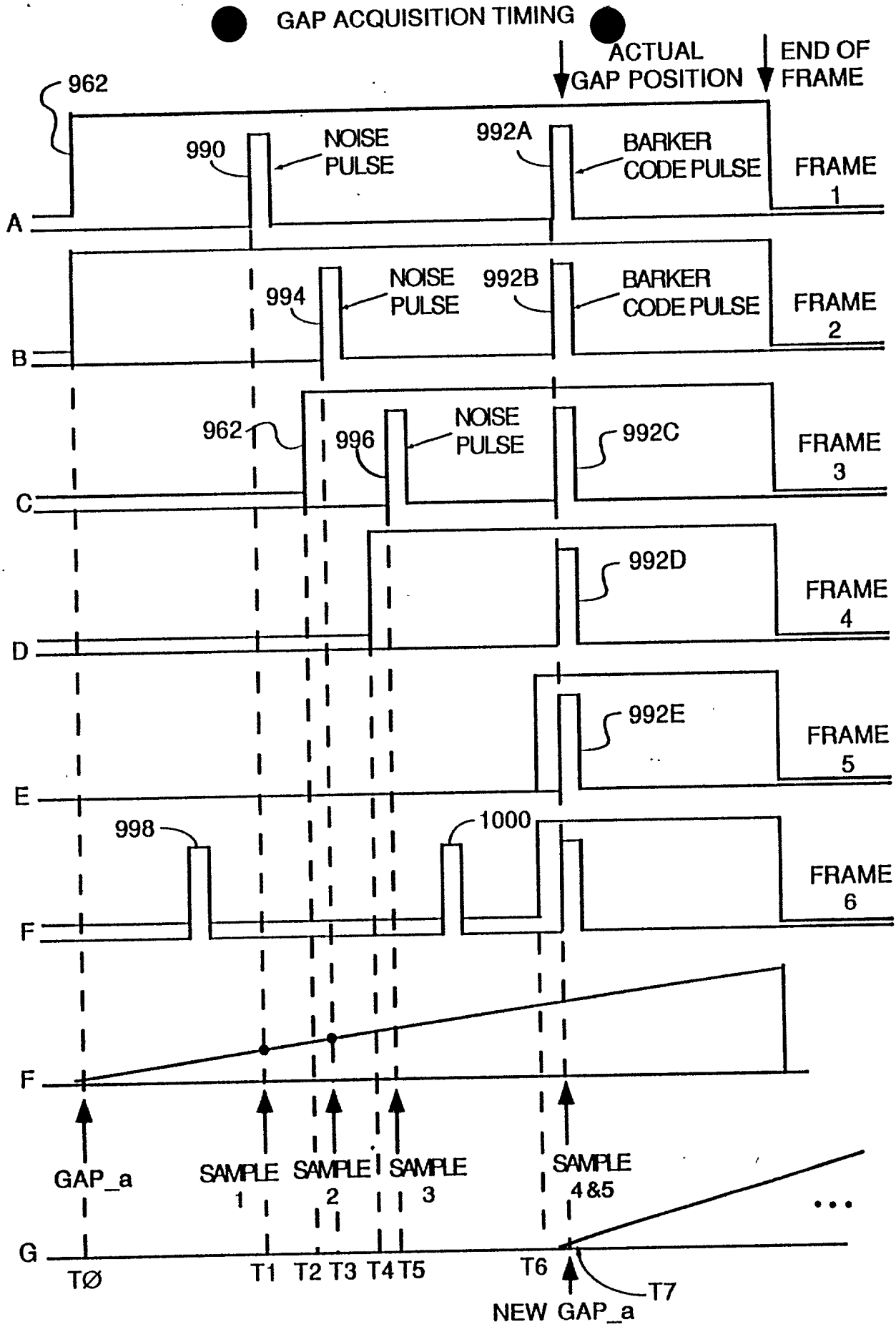
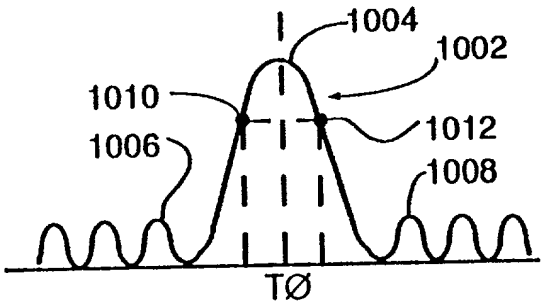
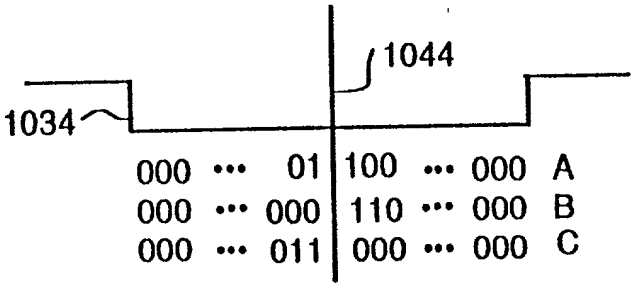

GAP ACQUISITION TIMING
ACTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4&5
G
TØ
T1 T2 T3 T4 T5
T6
T7
NEW GAP_a

FIG. 39 35



36

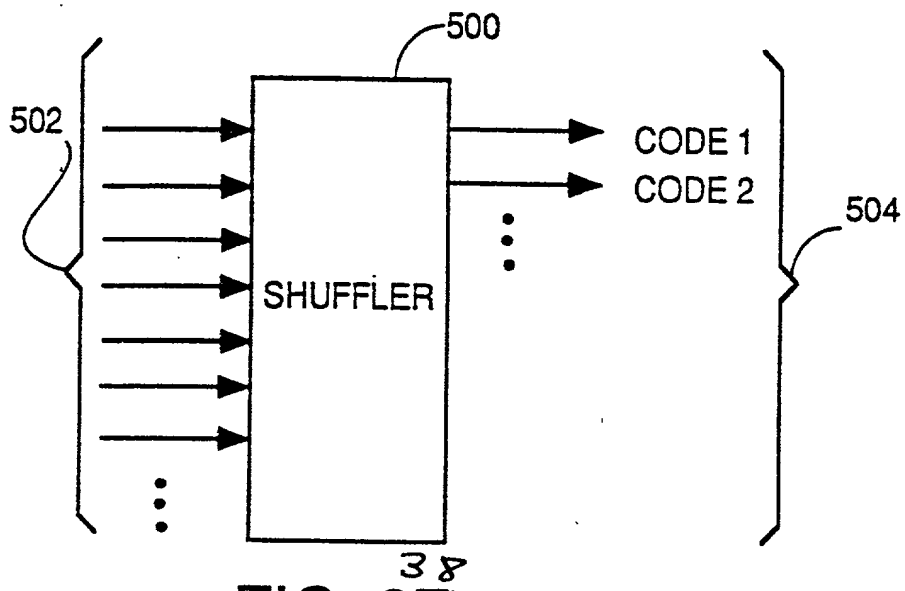
FIG. ~~40~~



37

FIG. ~~41~~

FINE TUNING TO CENTER BARKER CODE



38

FIG. 27

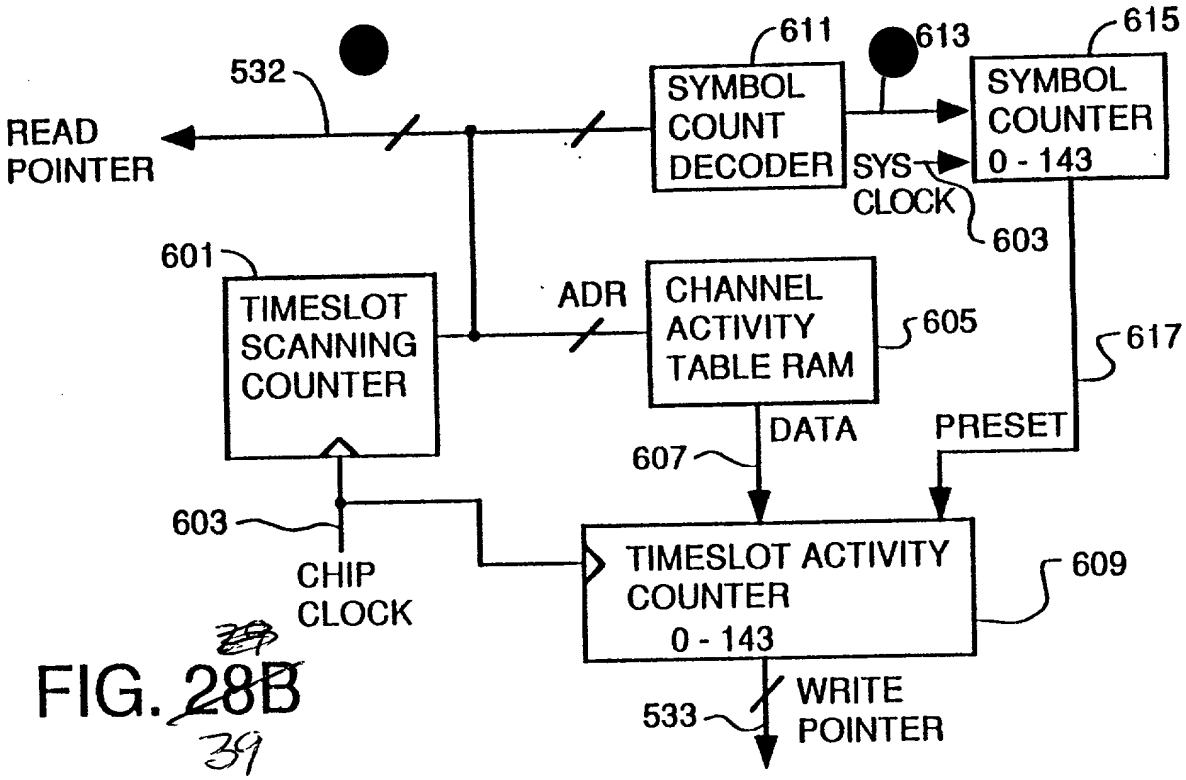


FIG. 28B

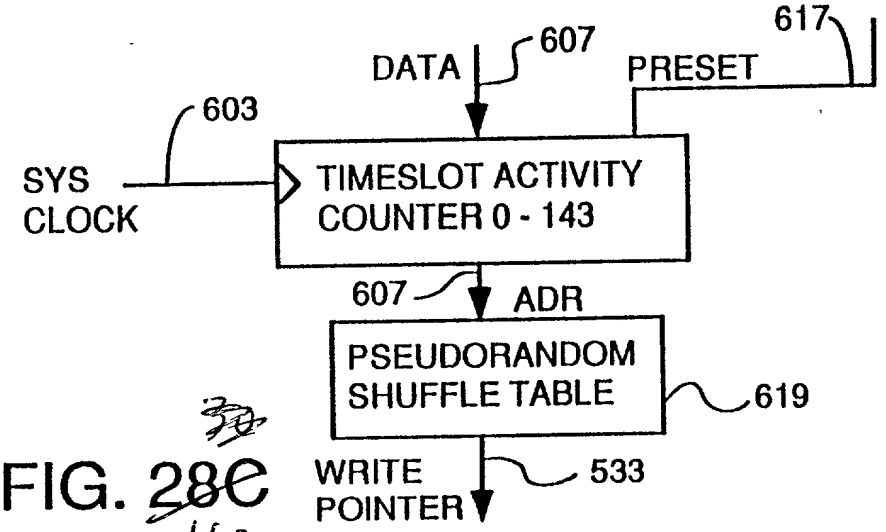


FIG. 28C

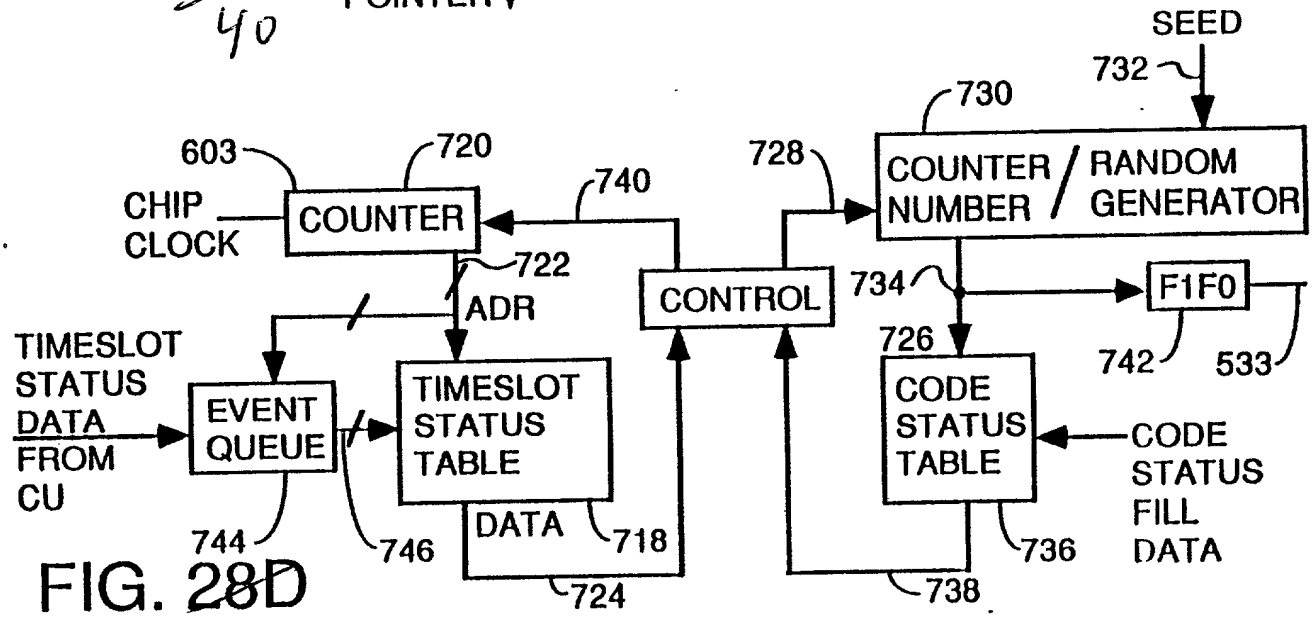
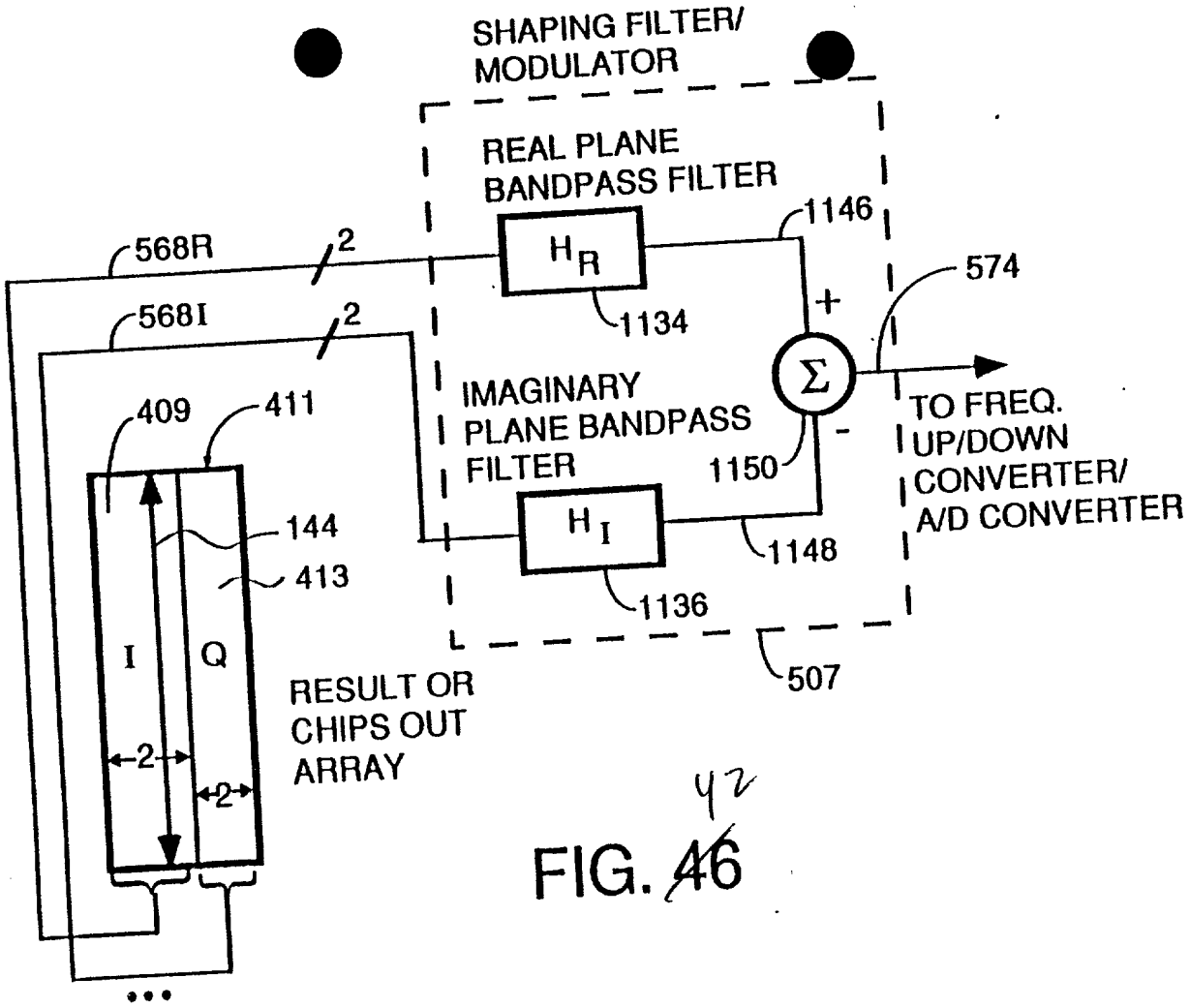
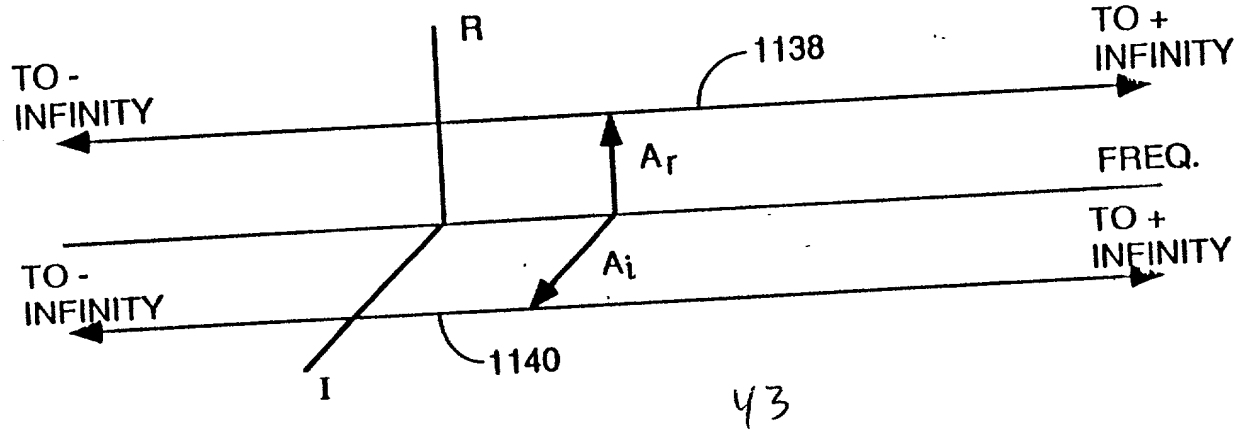


FIG. 28D



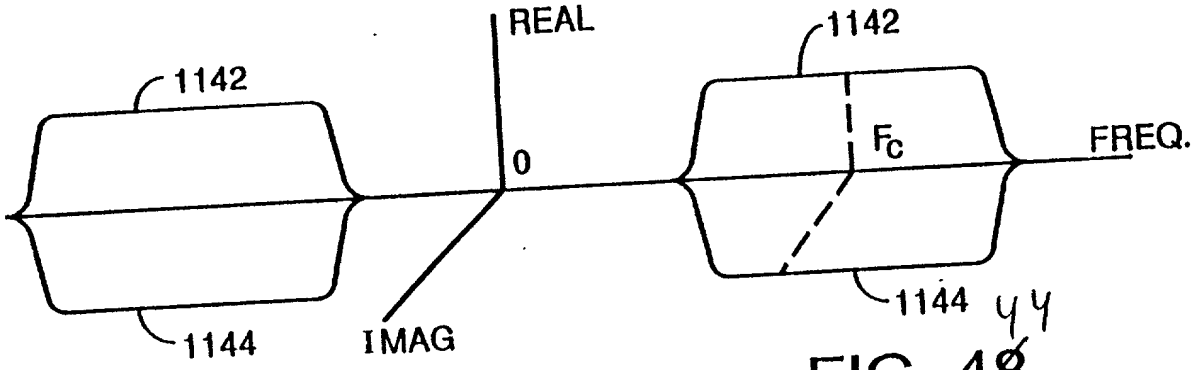
42

FIG. 46



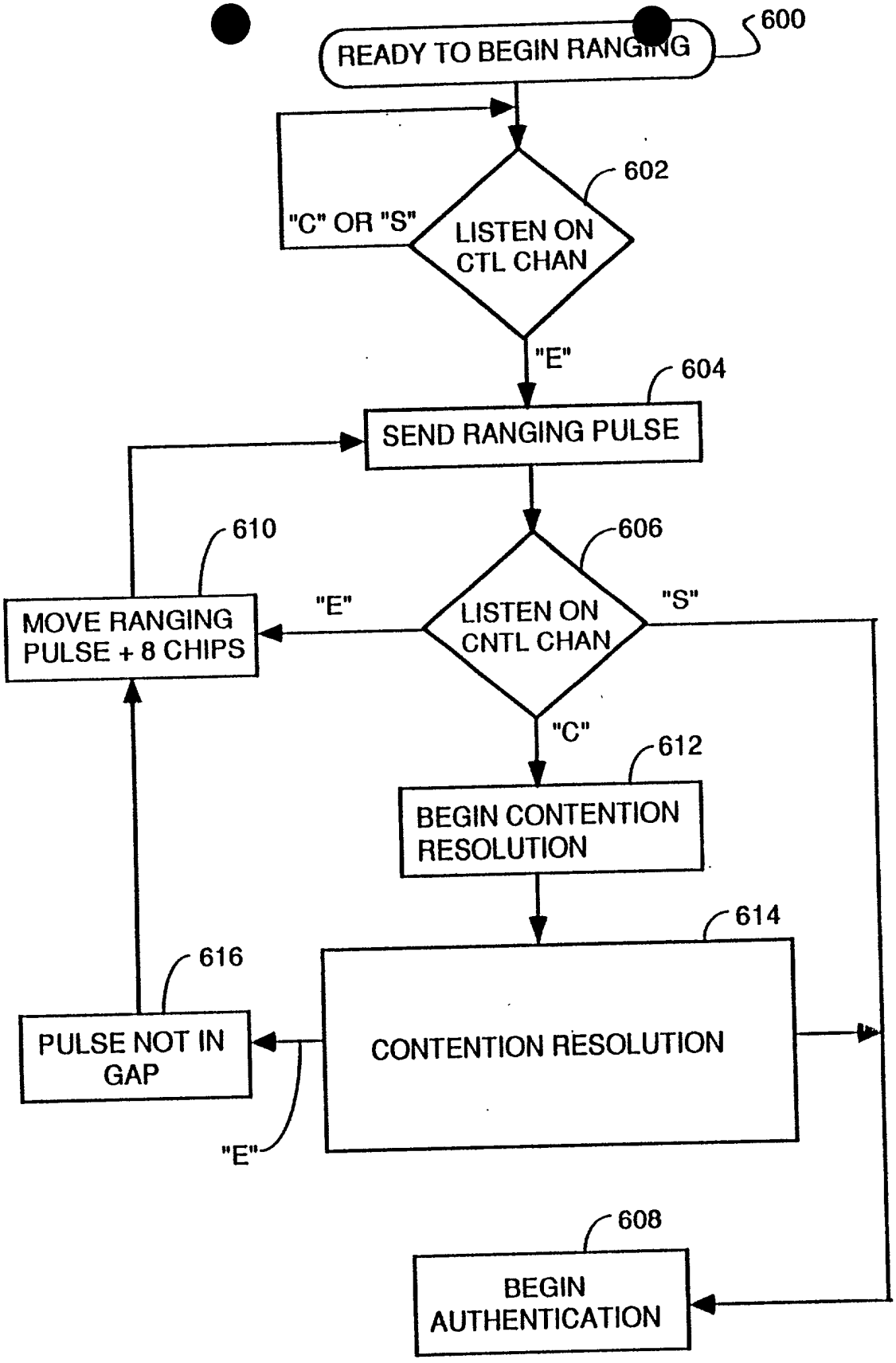
43

FIG. 47



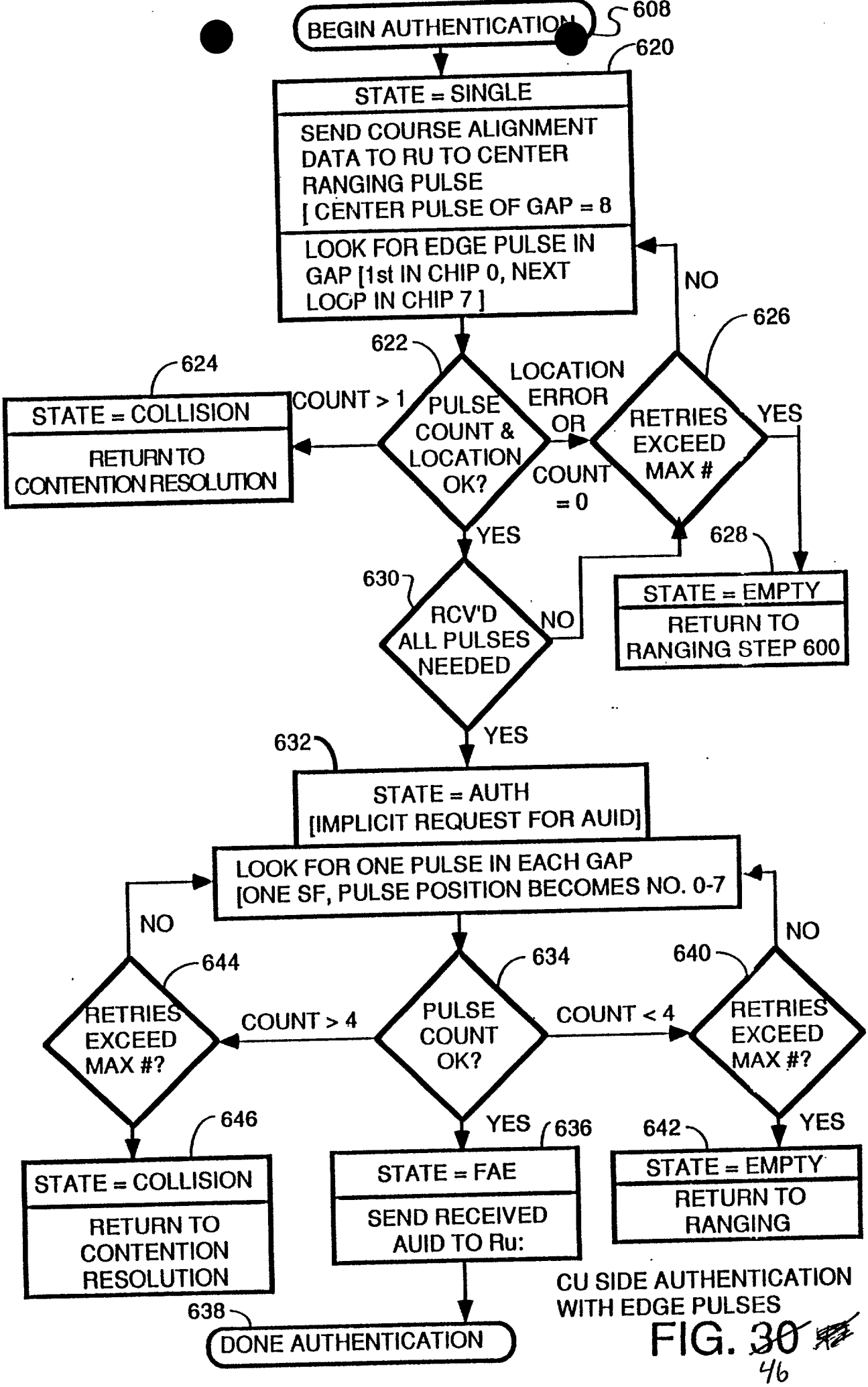
44

FIG. 48



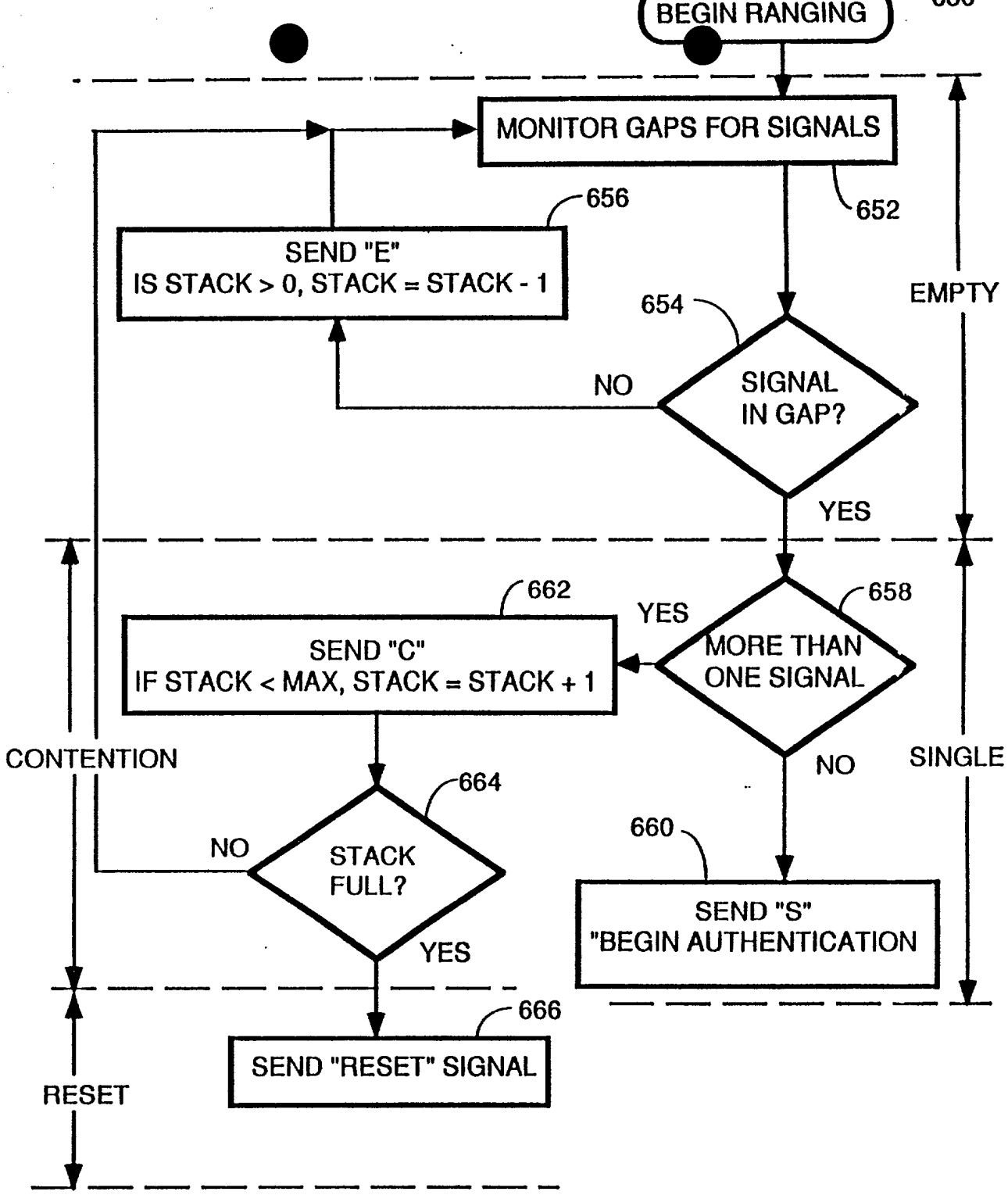
RU RANGING

FIG. 29



CU SIDE AUTHENTICATION WITH EDGE PULSES

FIG. 30



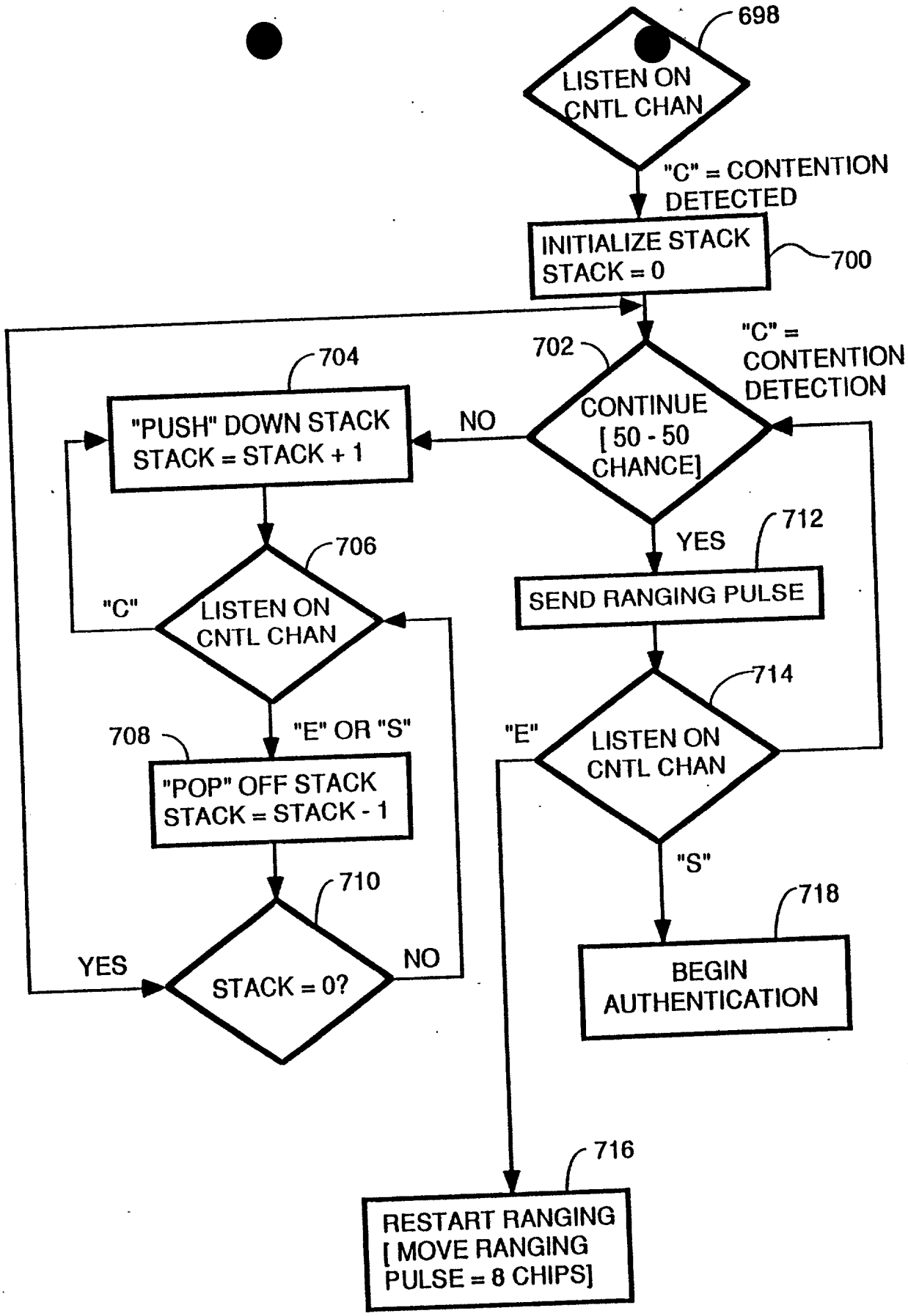
CU RANGING & CONTENTION RESOLUTION

~~RANGING AND CONTENTION RESOLUTION~~

~~CU SIDE~~

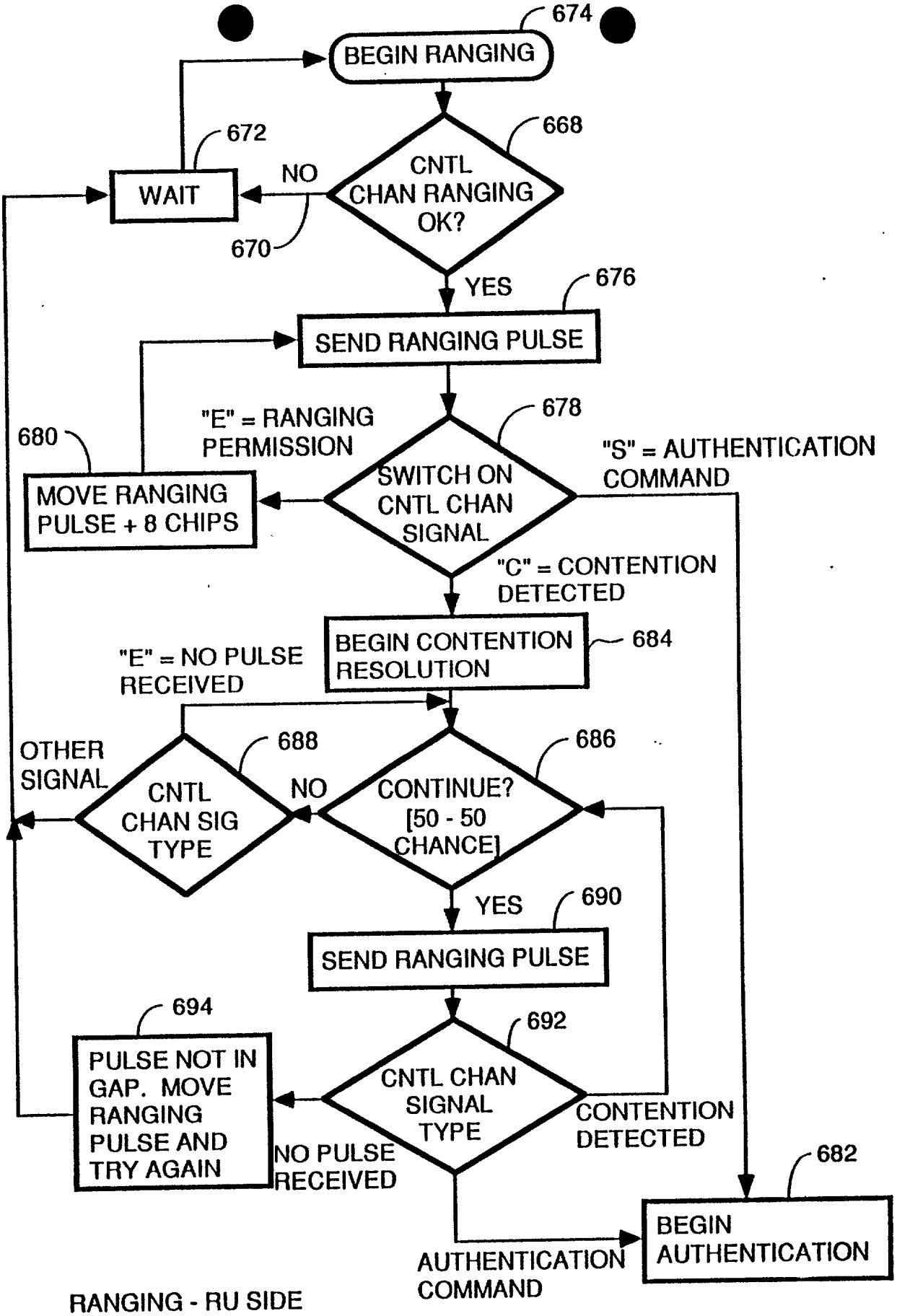
FIG. 31

47



CONTENTION RESOLUTION - RU USING BINARY STACK

FIG. 33



RANGING - RU SIDE
BINARY TREE
ALGORITHM

FIG. 32

50
49

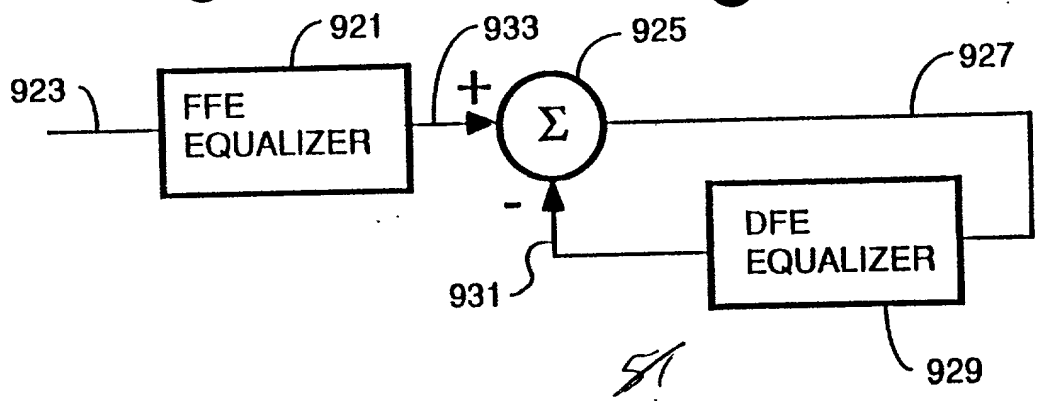


FIG. 37

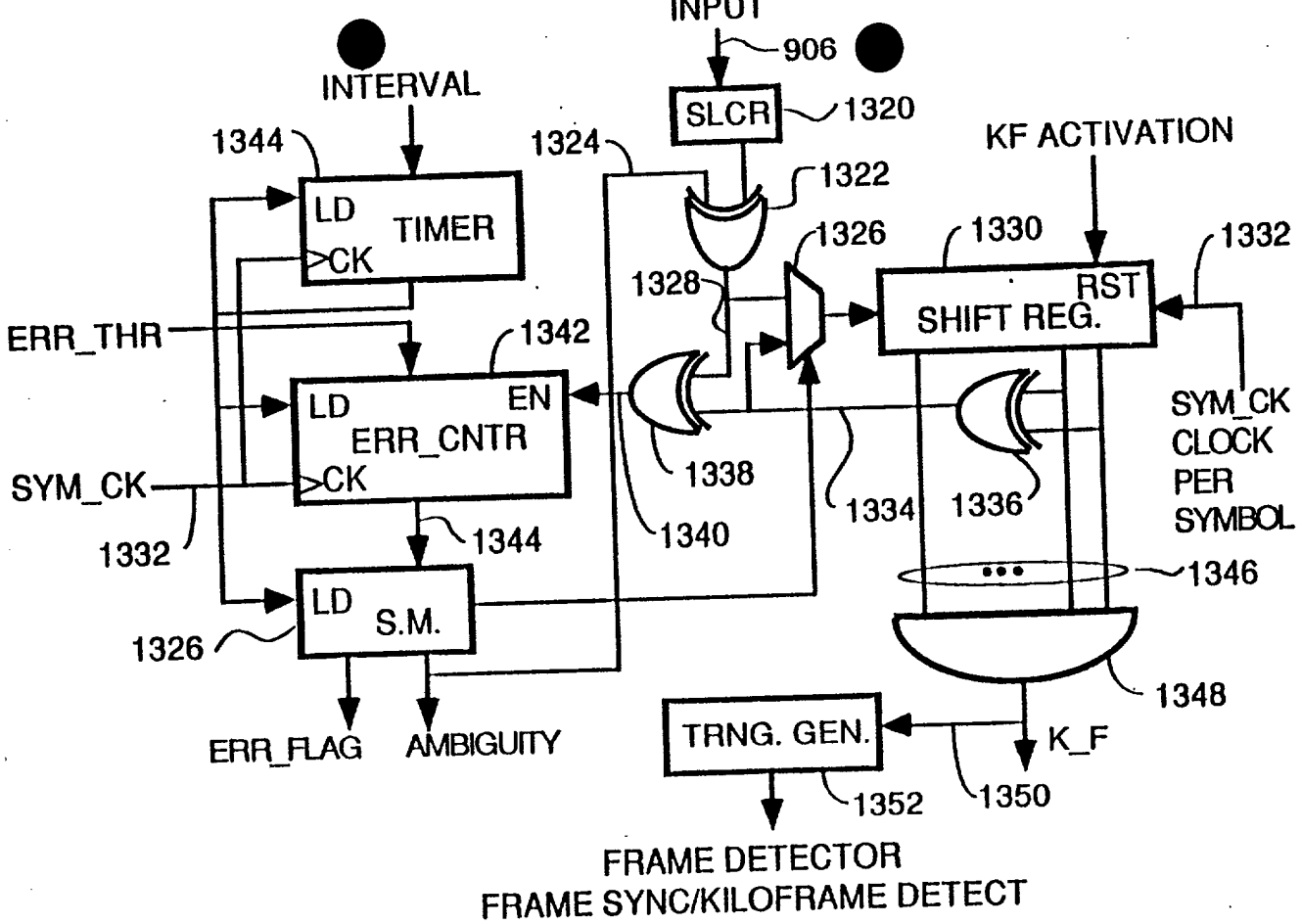
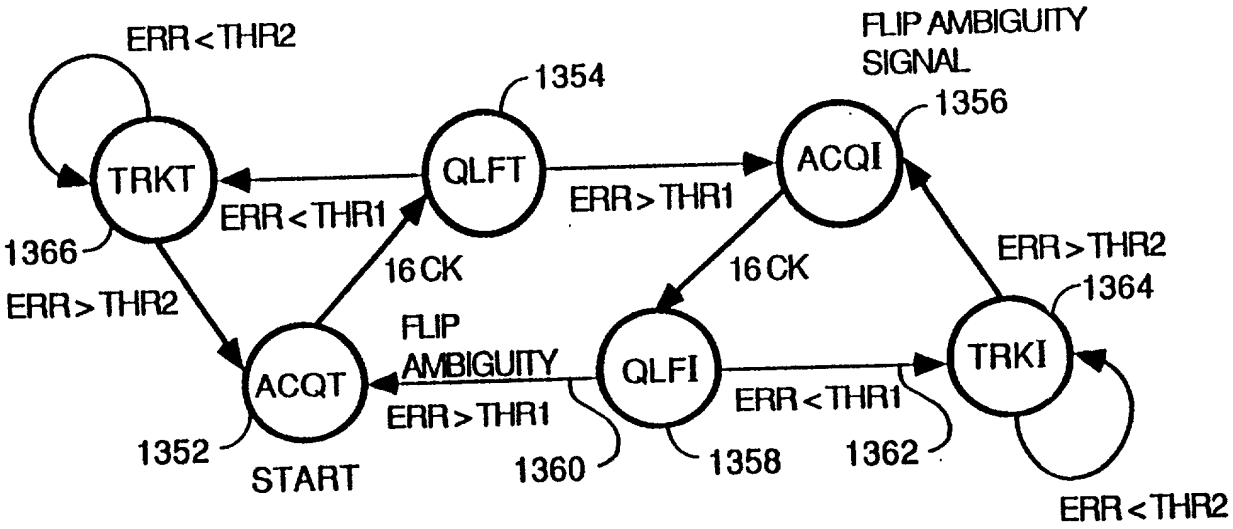


FIG. 52

51



STATE MACHINE

FIG. 53

52

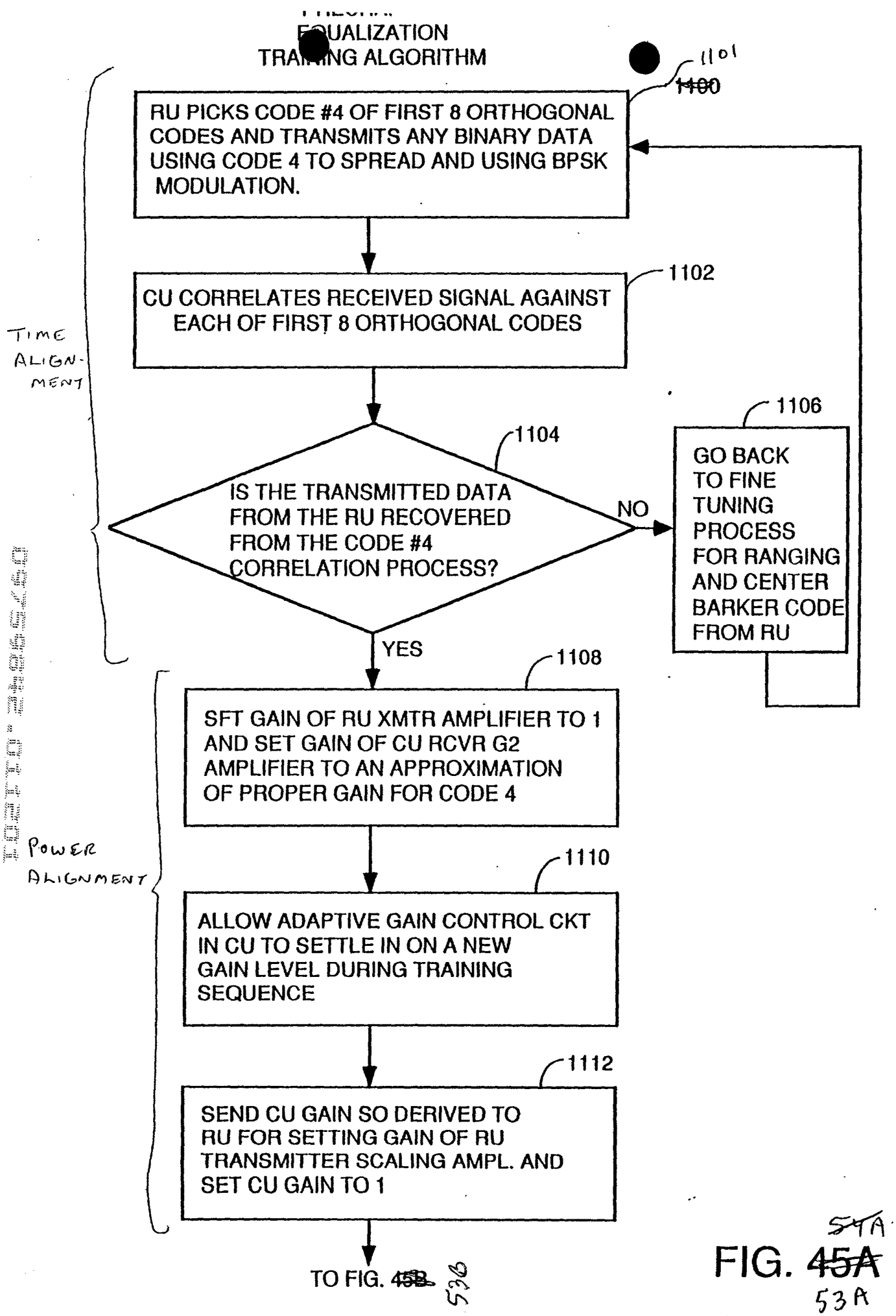

EQUALIZATION
TRAINING ALGORITHM
1101
1100
RU PICKS CODE #4 OF FIRST 8 ORTHOGONAL CODES AND TRANSMITS ANY BINARY DATA USING CODE 4 TO SPREAD AND USING BPSK MODULATION.
1102
CU CORRELATES RECEIVED SIGNAL AGAINST EACH OF FIRST 8 ORTHOGONAL CODES
TIME ALIGN-MENT
1104
IS THE TRANSMITTED DATA FROM THE RU RECOVERED FROM THE CODE #4 CORRELATION PROCESS?
NO
1106
GO BACK TO FINE TUNING PROCESS FOR RANGING AND CENTER BARKER CODE FROM RU
YES
1108
SFT GAIN OF RU XMTR AMPLIFIER TO 1 AND SET GAIN OF CU RCVR G2 AMPLIFIER TO AN APPROXIMATION OF PROPER GAIN FOR CODE 4
POWER ALIGNMENT
1110
ALLOW ADAPTIVE GAIN CONTROL CKT IN CU TO SETTLE IN ON A NEW GAIN LEVEL DURING TRAINING SEQUENCE
1112
SEND CU GAIN SO DERIVED TO RU FOR SETTING GAIN OF RU TRANSMITTER SCALING AMPL. AND SET CU GAIN TO 1
TO FIG. 45B
536

FIG. 45A
53A

UPSTREAM EQUALIZATION

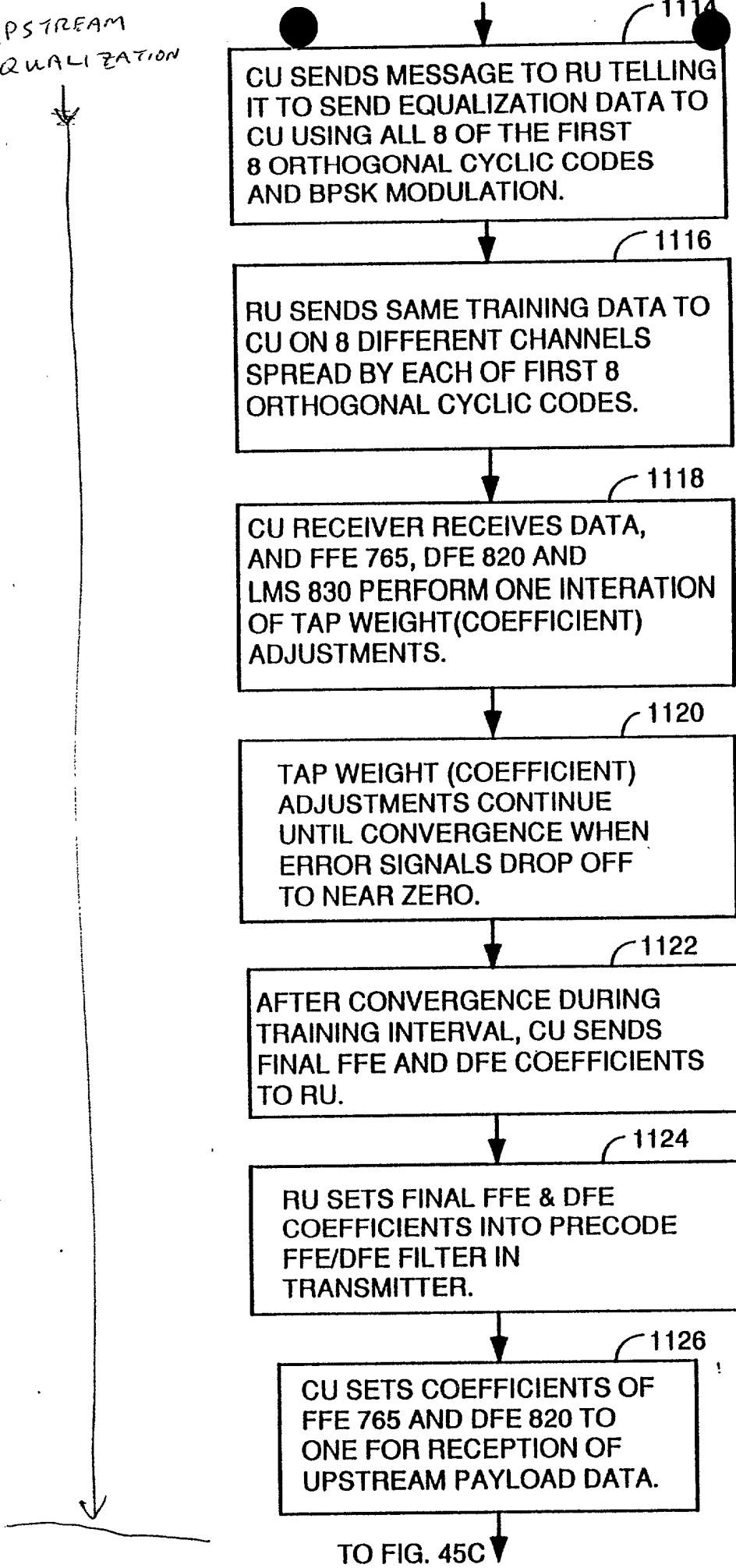


FIG. ~~45B~~ 54B
53B

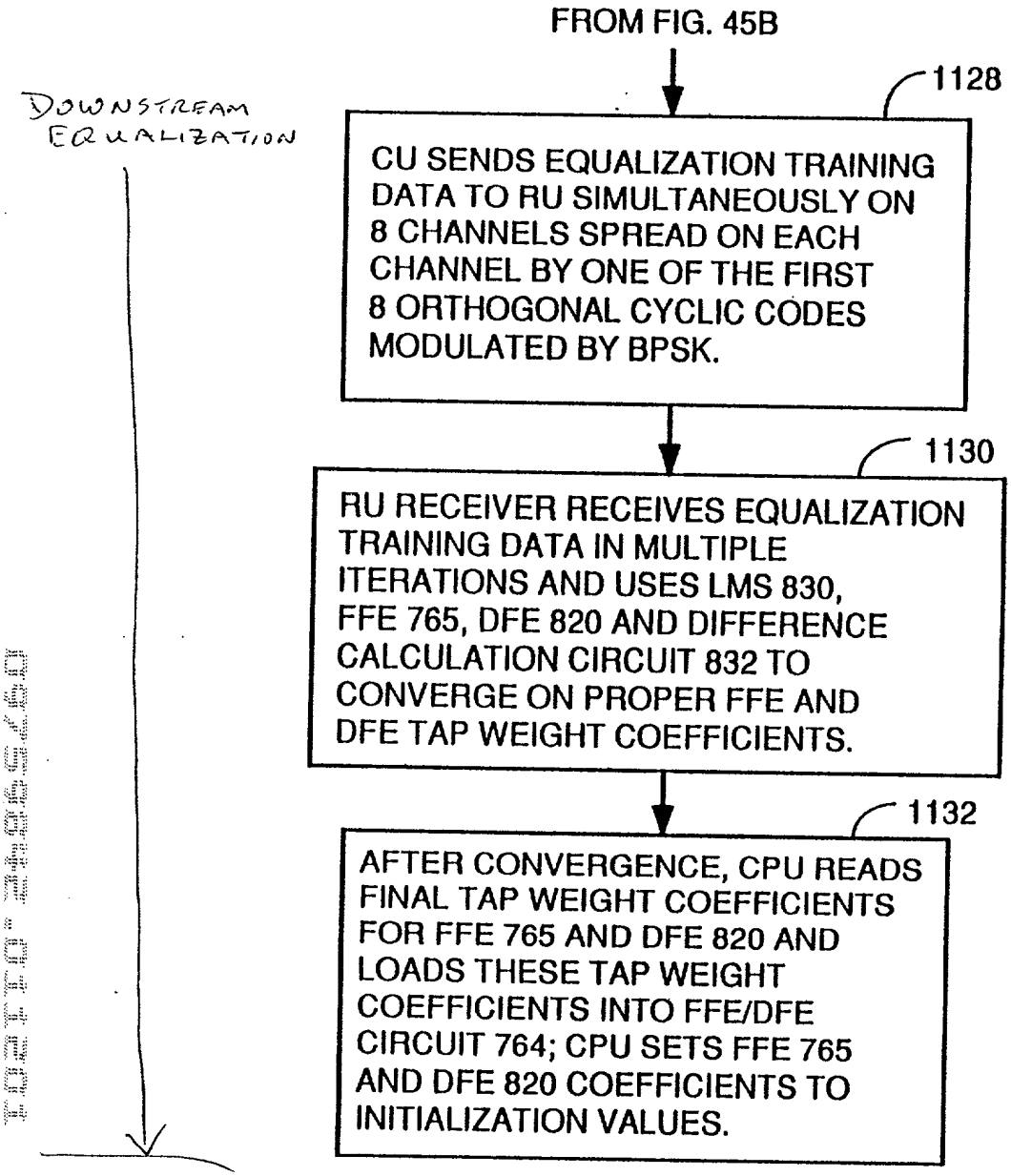

FROM FIG. 45B
DOWNSTREAM EQUALIZATION
1128
CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.
1130
RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.
1132
AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND LOADS THESE TAP WEIGHT COEFFICIENTS INTO FFE/DFE CIRCUIT 764; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

FIG. 45C

53C

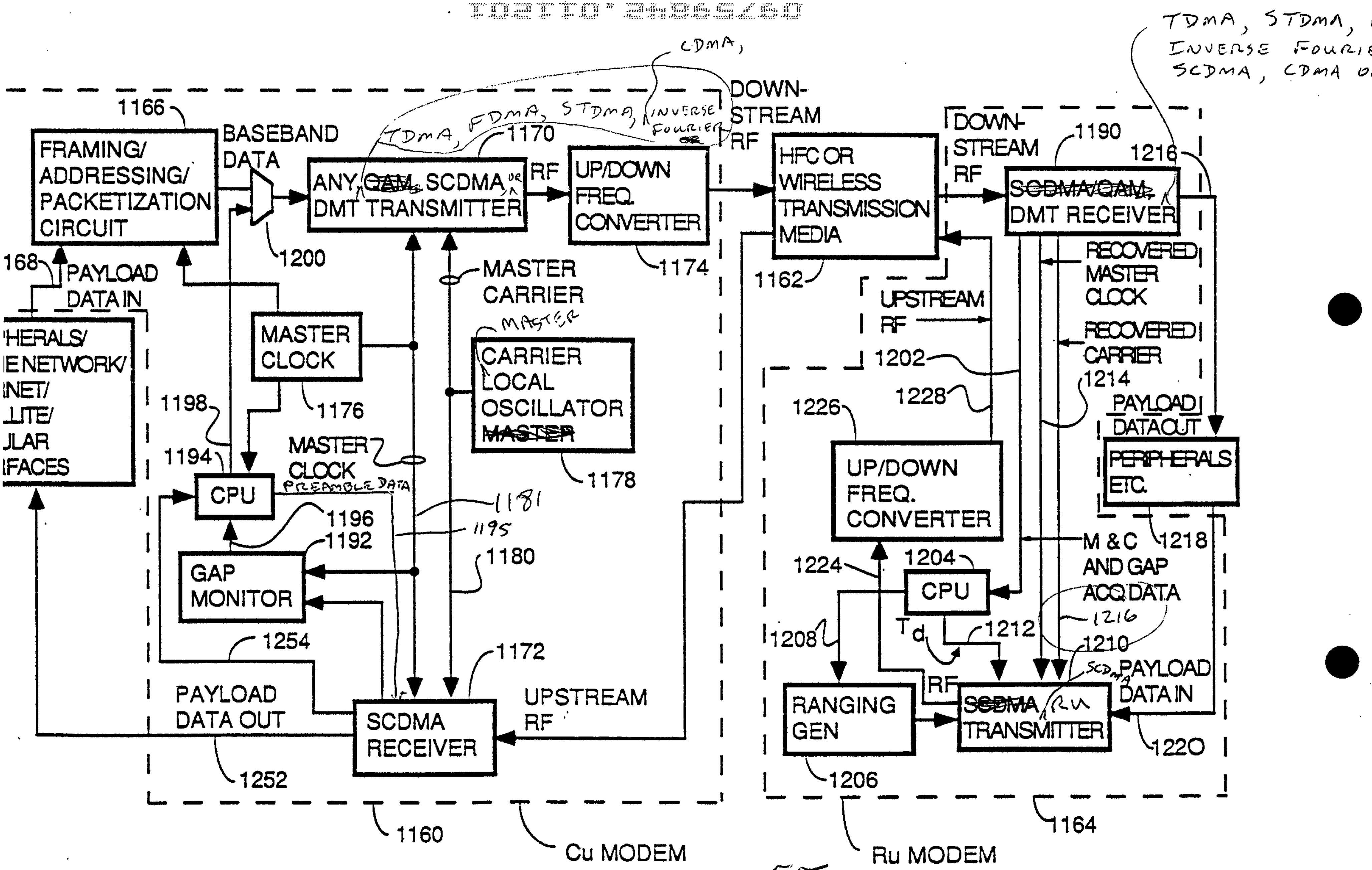
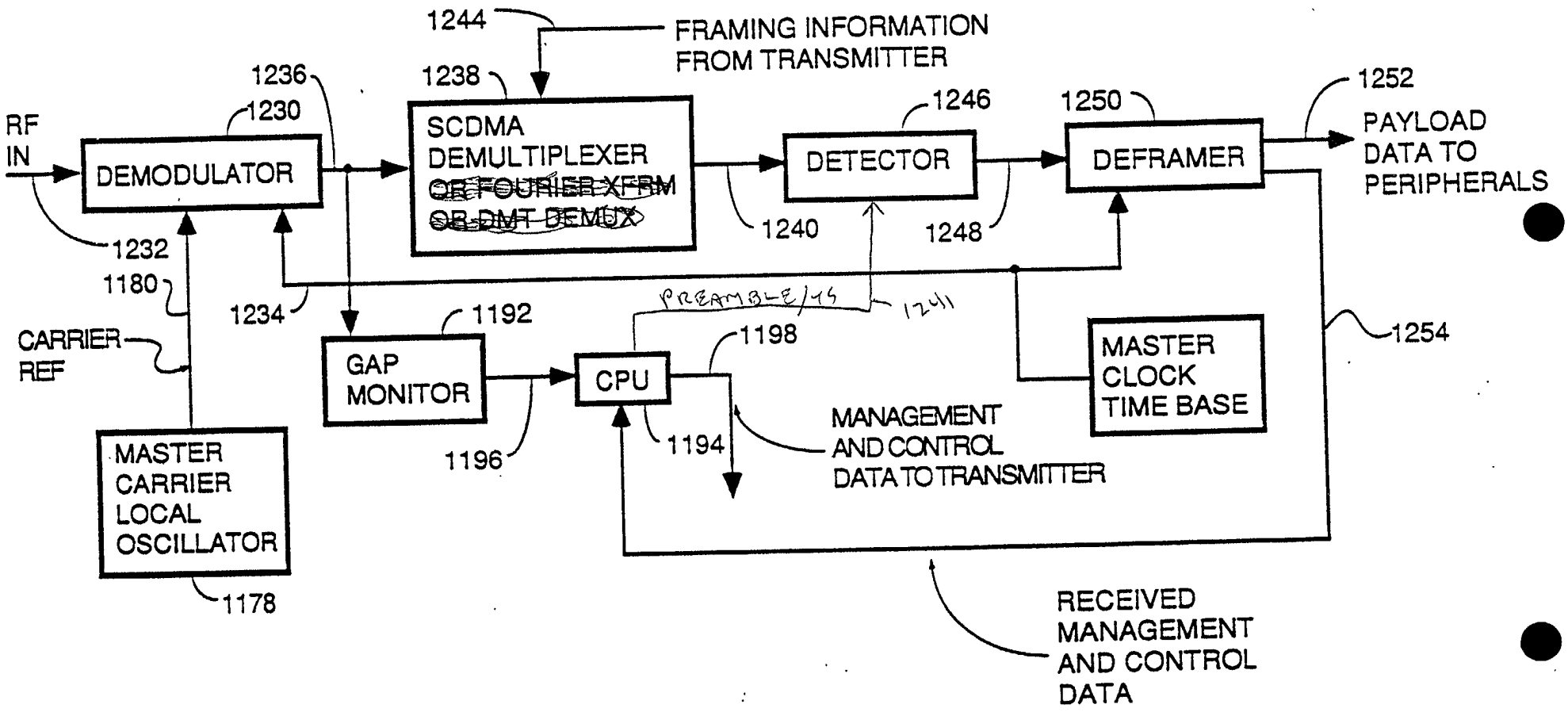

TDMA, STDMA,
INVERSE FOURIE
SCDMA, CDMA OR
CDMA,
1166
FRAMING/
ADDRESSING/
PACKETIZATION
CIRCUIT
BASEBAND
DATA
TDMA, FDMA, STDMA, INVERSE FOURIER OR
1170
ANY QAM, SCDMA
DMT TRANSMITTER
RF
UP/DOWN
FREQ.
CONVERTER
DOWN-
STREAM
RF
HFC OR
WIRELESS
TRANSMISSION
MEDIA
DOWN-
STREAM
RF
1190
1216
SCDMA/QAM
DMT RECEIVER
168
PAYLOAD
DATA IN
1200
MASTER
CARRIER
1174
1162
RECOVERED
MASTER
CLOCK
UPSTREAM
RF
RECOVERED
CARRIER
MASTER CLOCK
1176
MASTER
CARRIER
LOCAL
OSCILLATOR
MASTER
1202
1214
1198
1228
1226
PAYLOAD
DATA OUT
1194
MASTER
CLOCK
PREAMBLE DATA
UP/DOWN
FREQ.
CONVERTER
PERIPHERALS
ETC.
CPU
1178
1181
1196
1195
1192
M & C
AND GAP
ACQ DATA
1218
1180
1224
1204
GAP
MONITOR
CPU
1216
1208
T_d
1212
1210
1254
1172
RF
SCDMA
PAYLOAD
DATA IN
PAYLOAD
DATA OUT
SCDMA
RECEIVER
UPSTREAM
RF
RANGING
GEN
SCDMA Ru
TRANSMITTER
1220
1252
1206
1160
1164
Cu MODEM
Ru MODEM

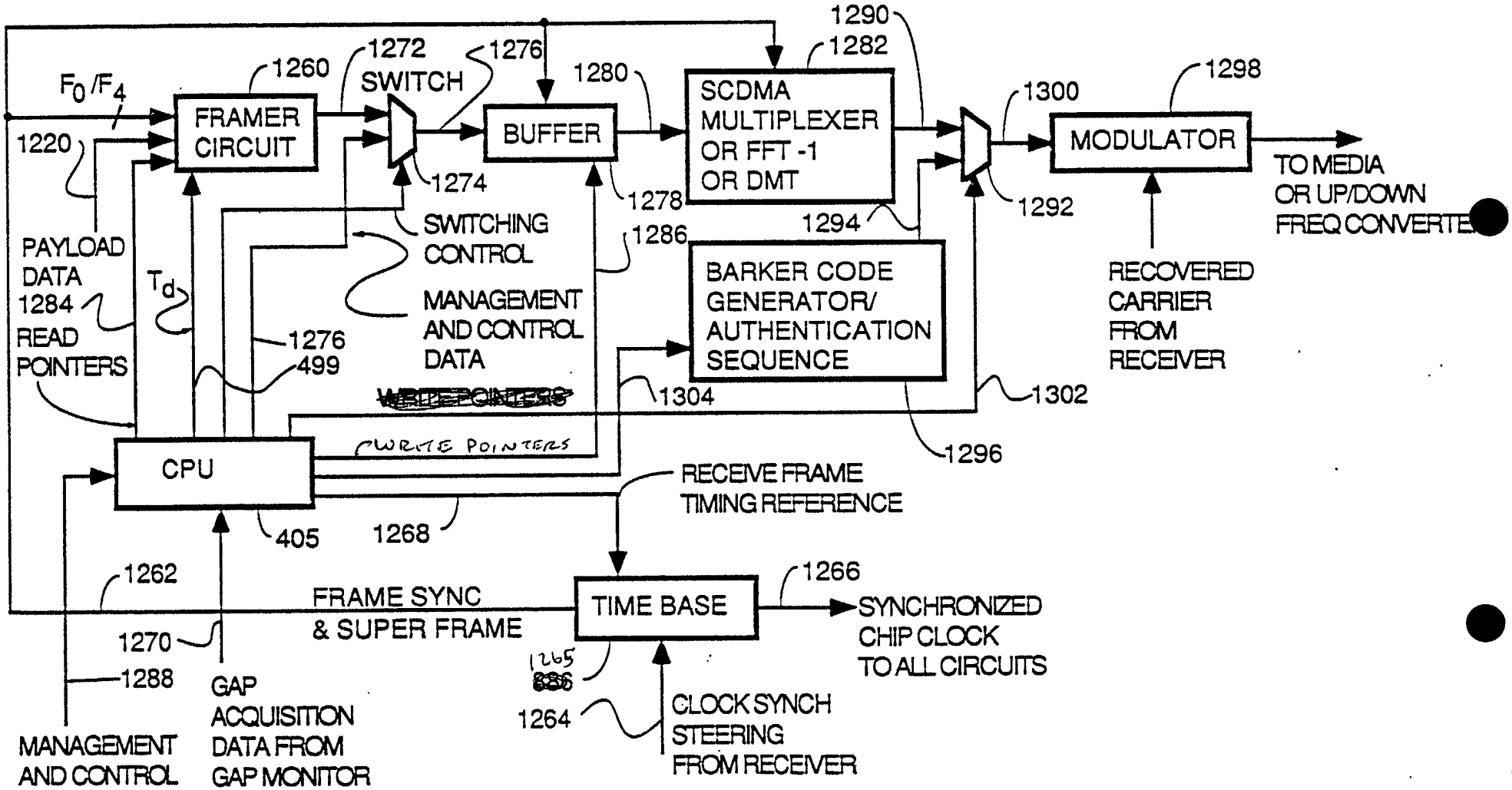
FIG. ~~49~~ ~~55~~ 54



SIMPLE Cu SPREAD SPECTRUM RECEIVER

FIG. ~~50~~ 56

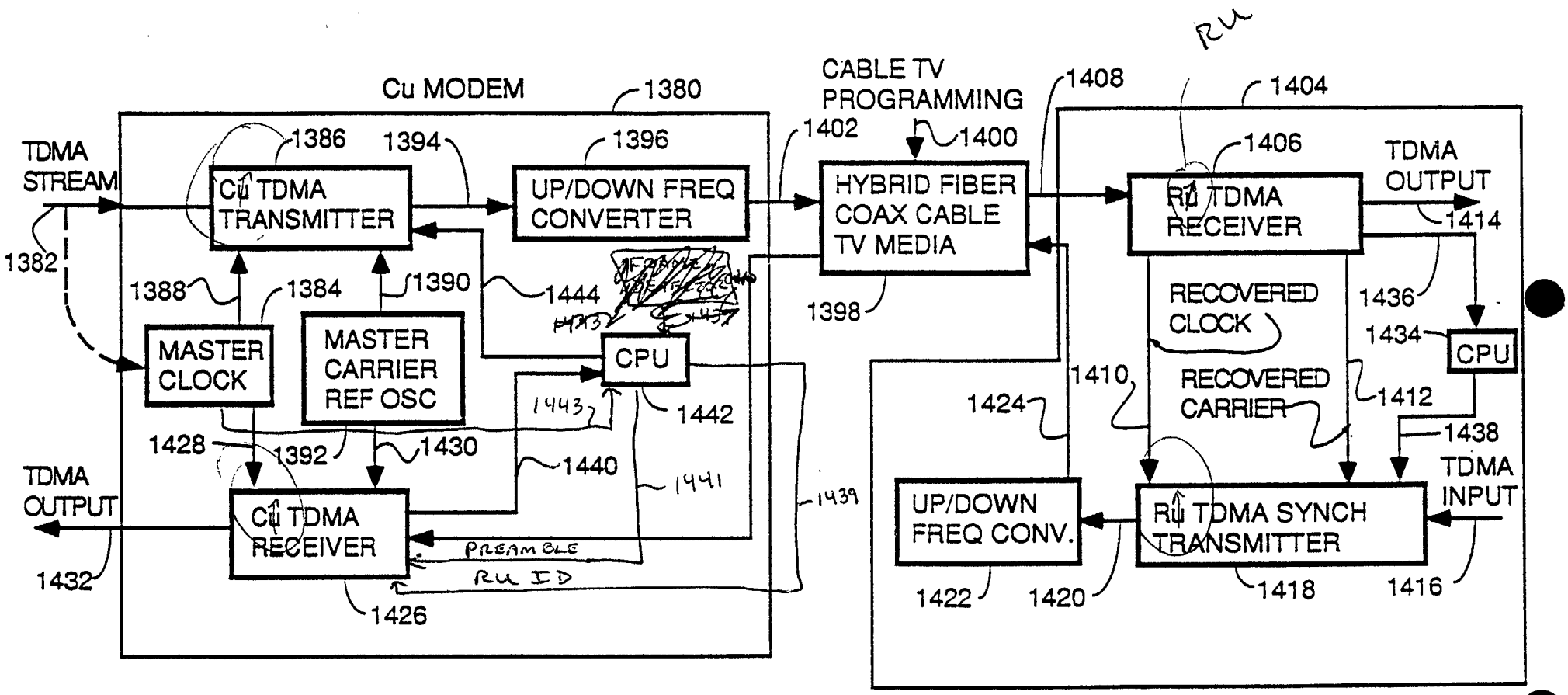
55



SIMPLE Ru SPREAD SPECTRUM TRANSMITTER

FIG. 51

56



SYNCHRONOUS TDMA SYSTEM

FIG. 54

57

OFFSET	1B ASIC		2A ASIC	
(Chips)	RGSRH	RGSRL	RGSRH	RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

Training Algorithm

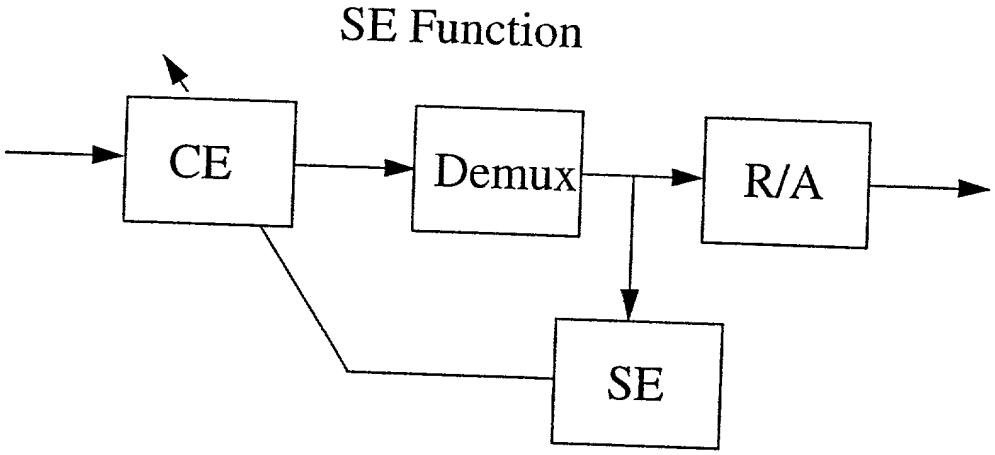
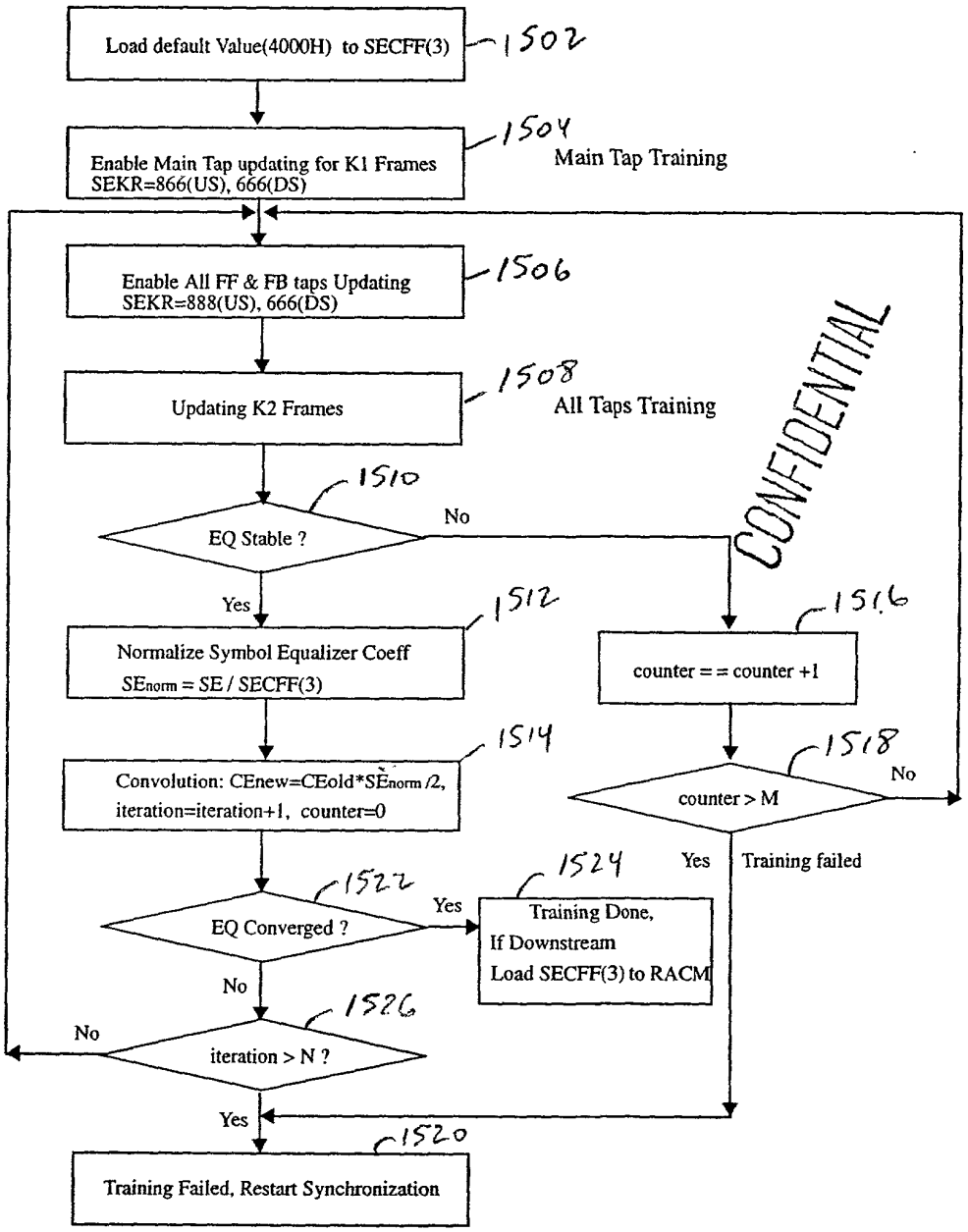


FIG. 59

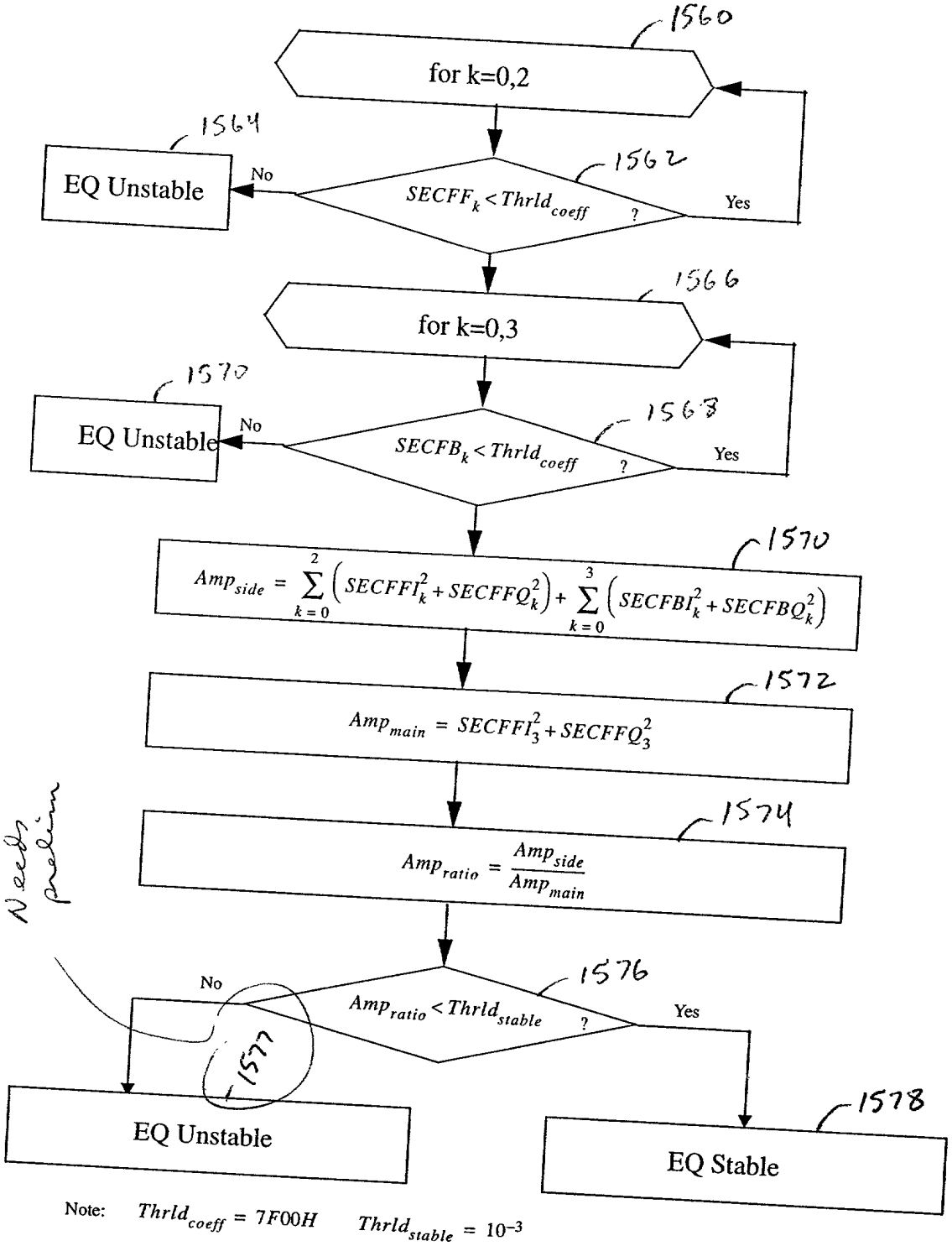
Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

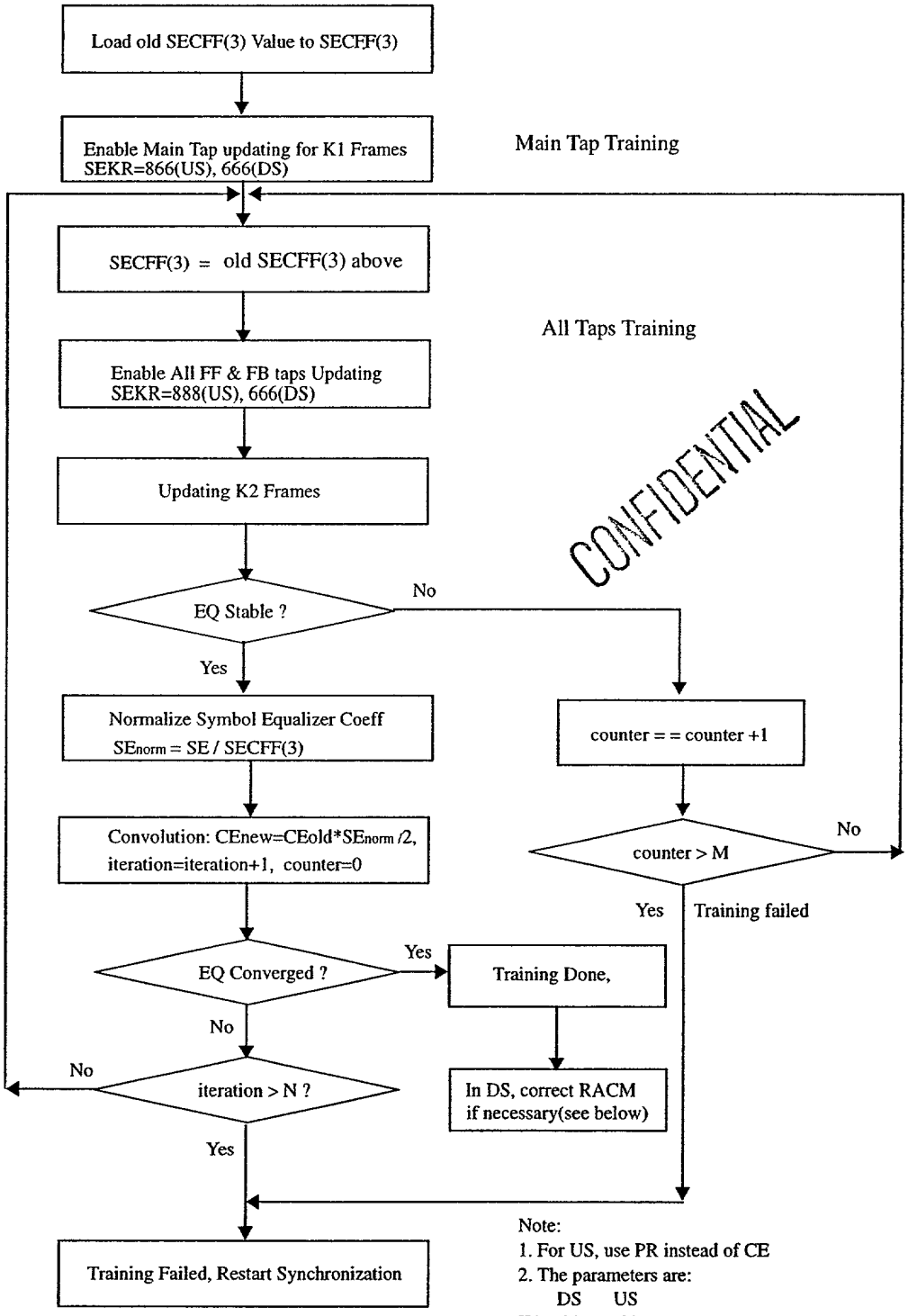
EQ Stability Check



Note: $Thrld_{coeff} = 7F00H$ $Thrld_{stable} = 10^{-3}$

FIG. 61

Periodic 2-Step Training Algorithm

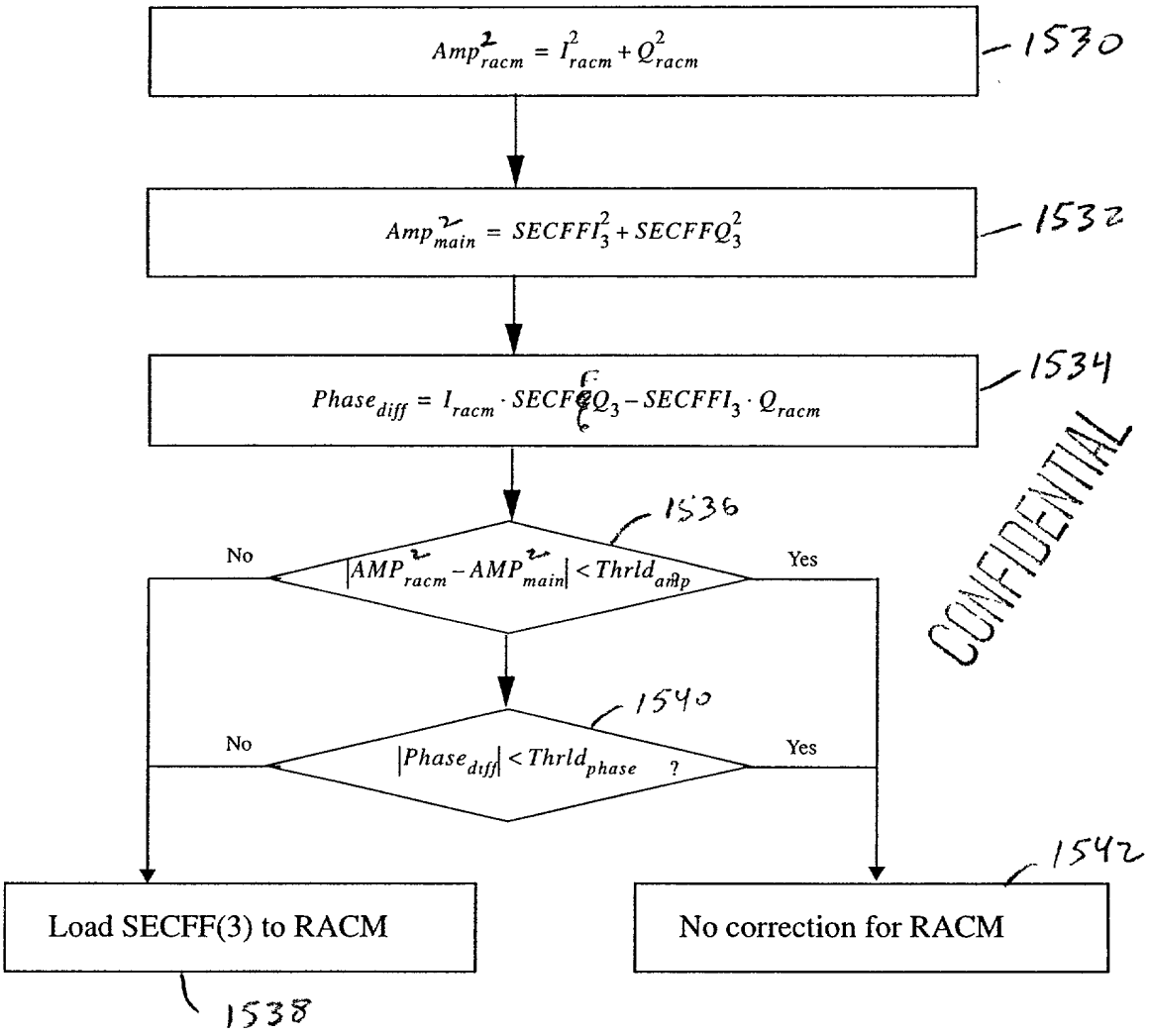


Note:
1. For US, use PR instead of CE
2. The parameters are:

	DS	US
K1	30	30
K2	20	30
N	5	3
M	3	3

FIG. 62

RACM Correction



CONFIDENTIAL

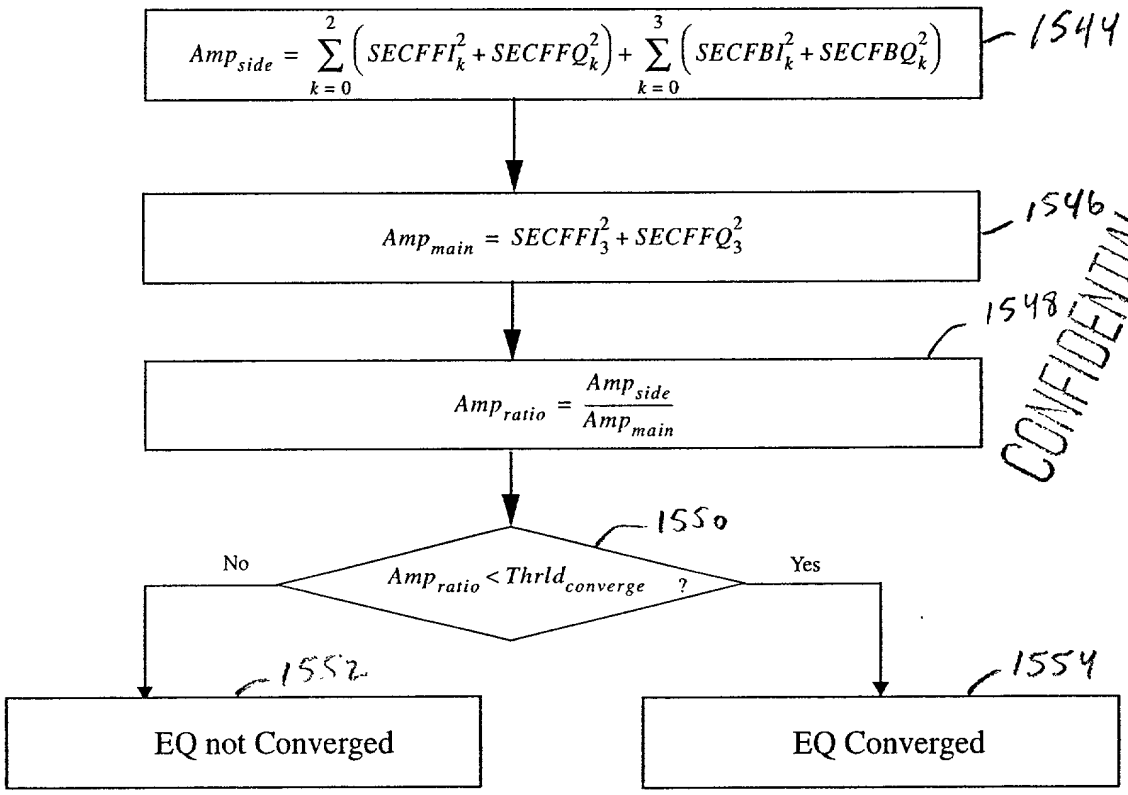
Note: $Thrld_{amp} = TBD$

$Thrld_{phase} = TBD$

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63.

EQ Convergence Check



Note: $Thrld_{converge} = 10^{-5}$

FIG. 64

Power Alignment Flow Chart

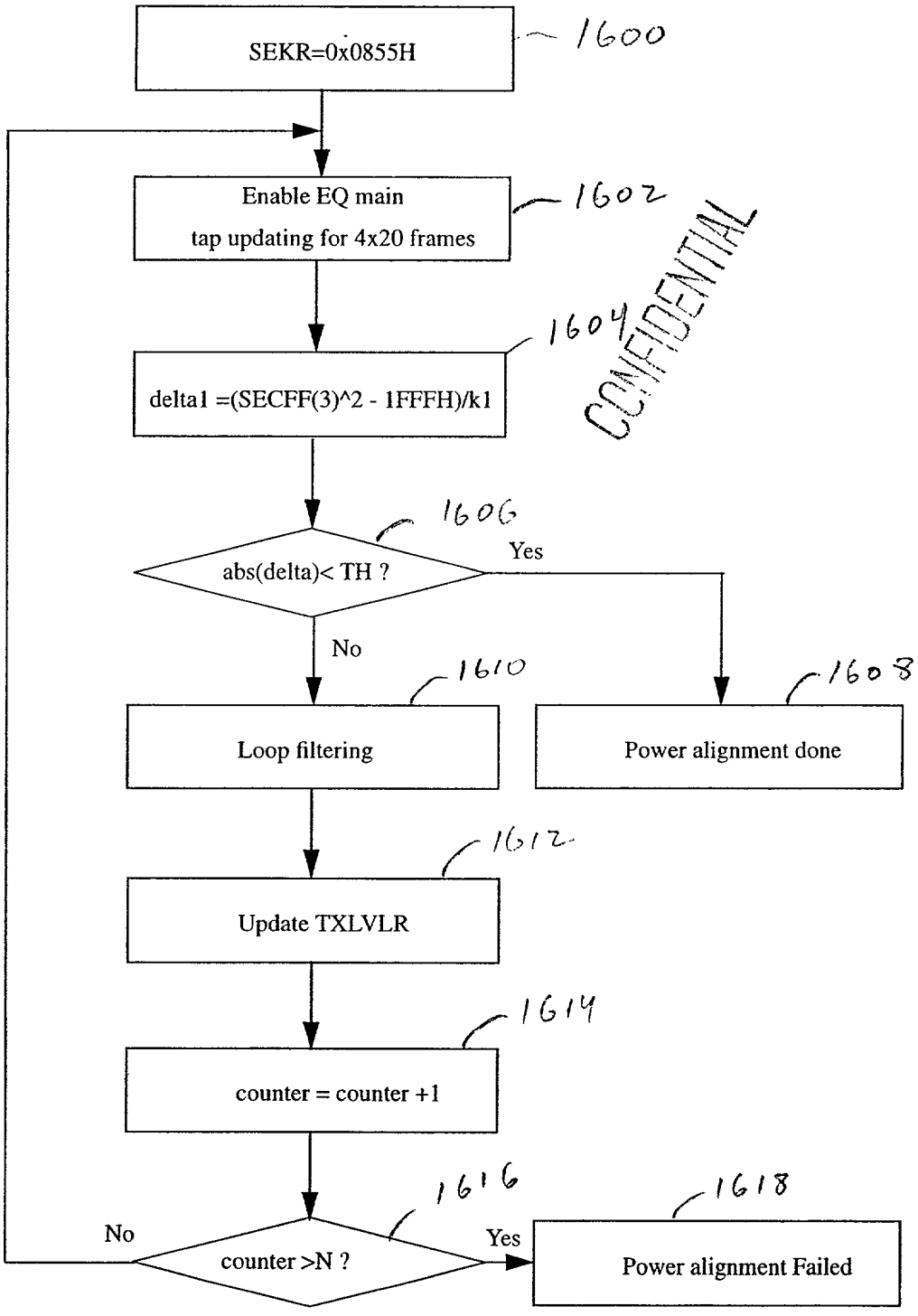


FIG. 65

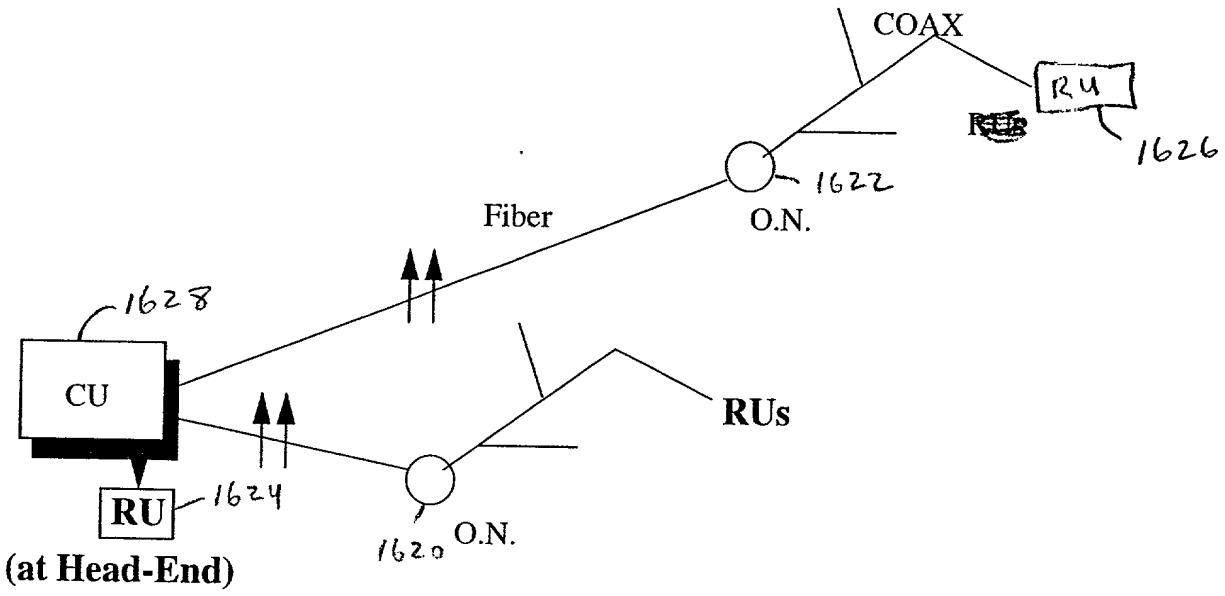
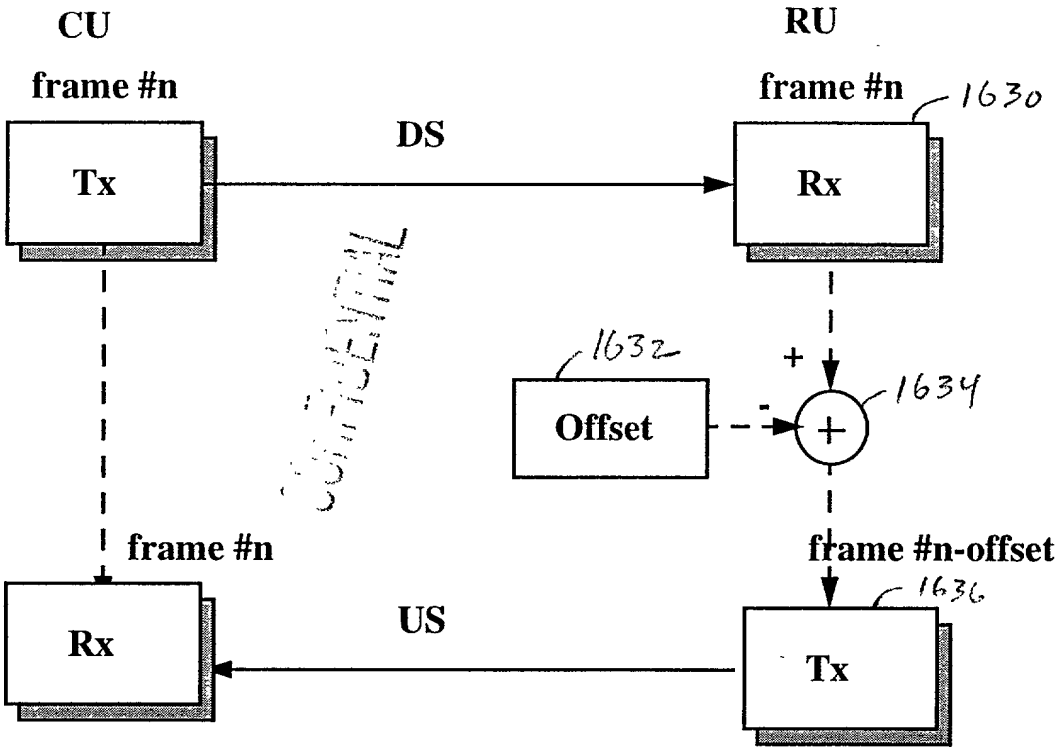


FIG. 66



Total Turn Around (TTA) in frames = Offset

FIG. 67

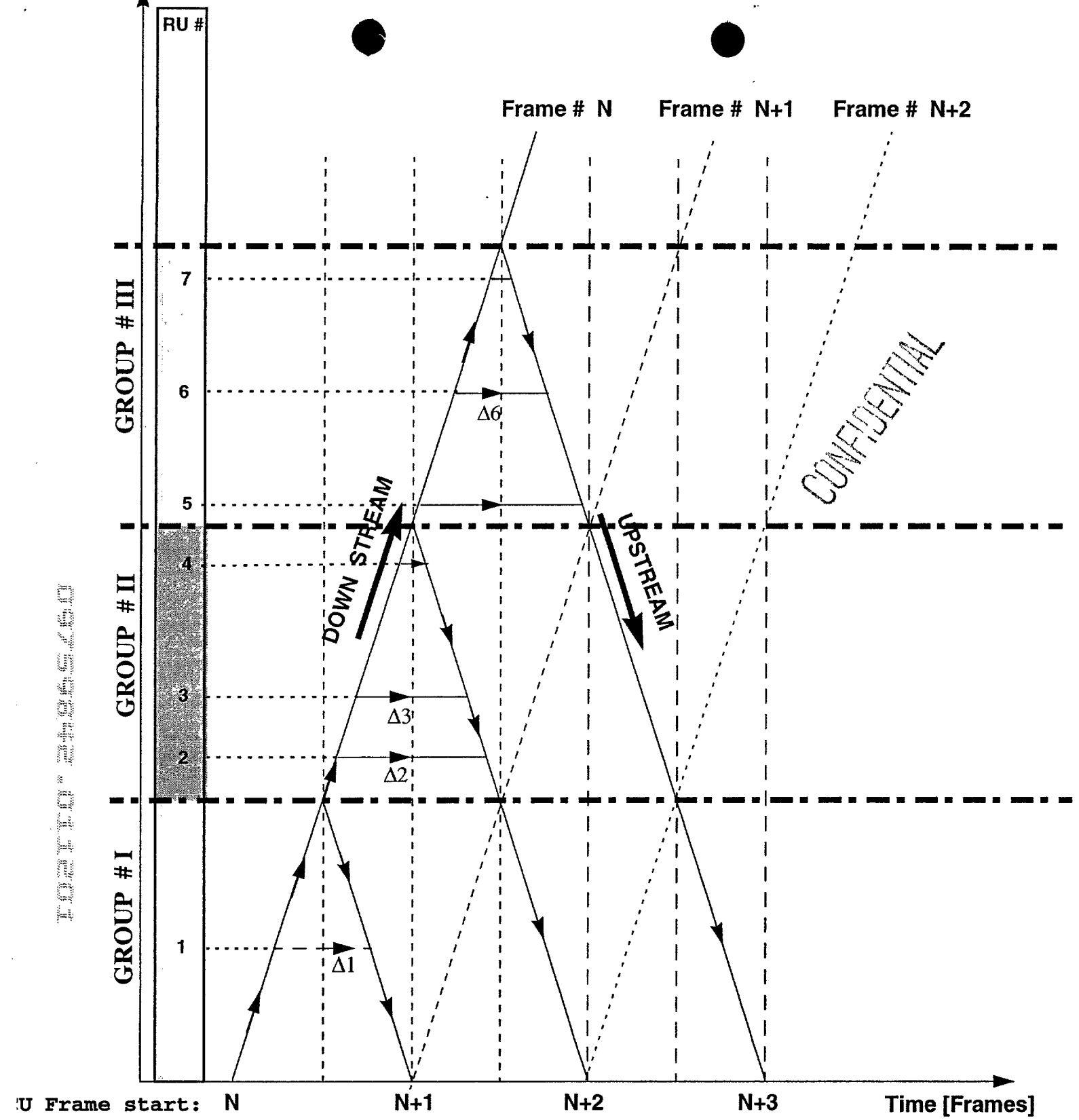


FIG. 68

Figure 3.1: Frame start propagation along the channel

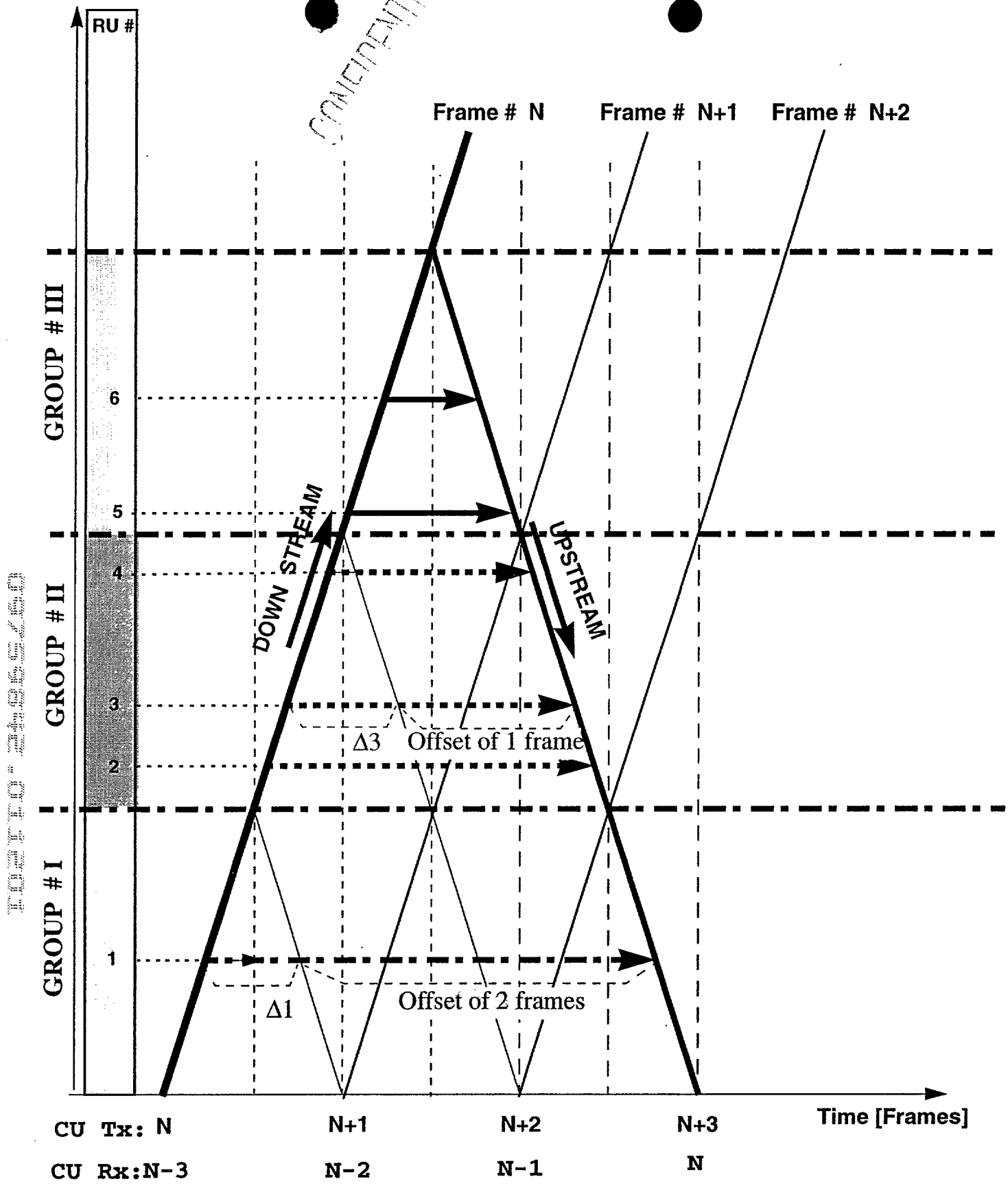


FIG. 69

Figure 69 Control message (downstream) and function (upstream) propagation in a 3 frames TTA channel

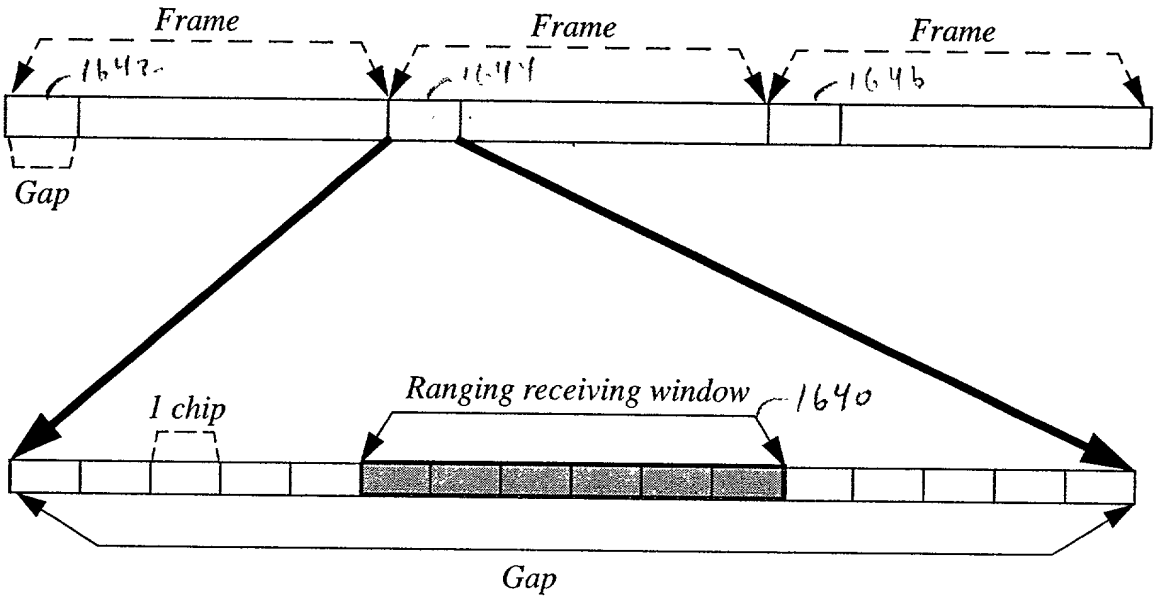


FIG. 70

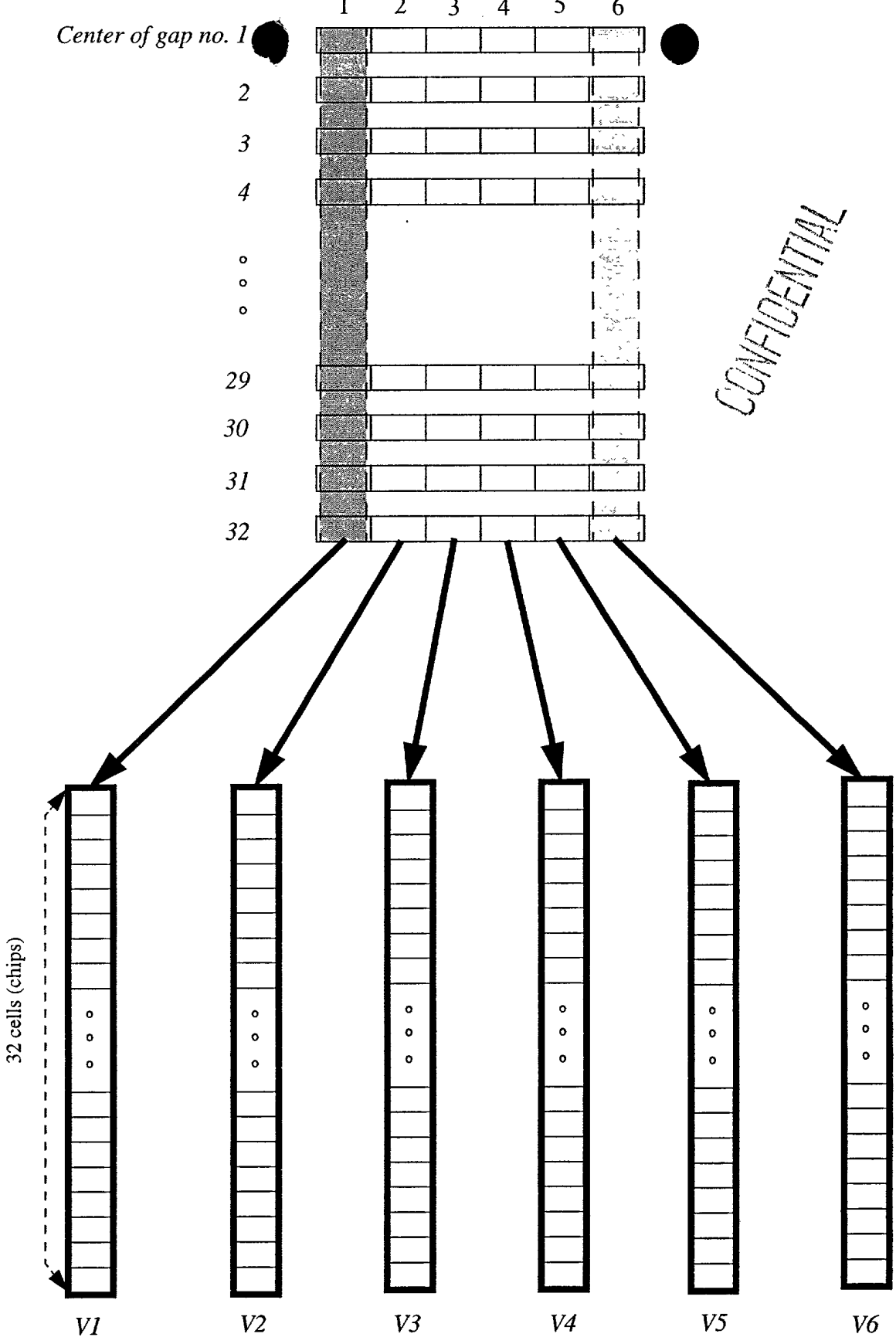


Figure 3.4: Overall view of the CU sensing windows in a "boundless ranging" algorithm

FIG. 71

Chip\FR	**1**	**2**	**3**	**4**	**5**	**6**	**7**		**33**
1	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**...**	**0**
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72

UPSTREAM EQUALIZATION

CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.

1116

RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.

1118

CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.

1120

TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.

1122

AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.

IN CU

1124

CONVOLVED SE CIRCUIT

~~RU~~ SETS FINAL FFE & DFE WITH OLD COEFFICIENTS ~~INTO~~ PRECODE FFE/DFE FILTER IN TRANSMITTER AND LOAD NEWLY CALCULATED COEFFICIENTS INTO RU XMTR PRECODE FILTER

RU

TRANSPARENCY VALUES

1126

CU SETS COEFFICIENTS OF FFE 765 AND DFE 820 TO ~~CU~~ FOR RECEPTION OF UPSTREAM PAYLOAD DATA.

TO FIG. 45C

54B

FIG. 45B

53B

FAXED TO
DI MUELLER
10/25/00
(909) 596-3733

FROM FIG. 45B

DOWNSTREAM EQUALIZATION

1128

CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.

1130

RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.

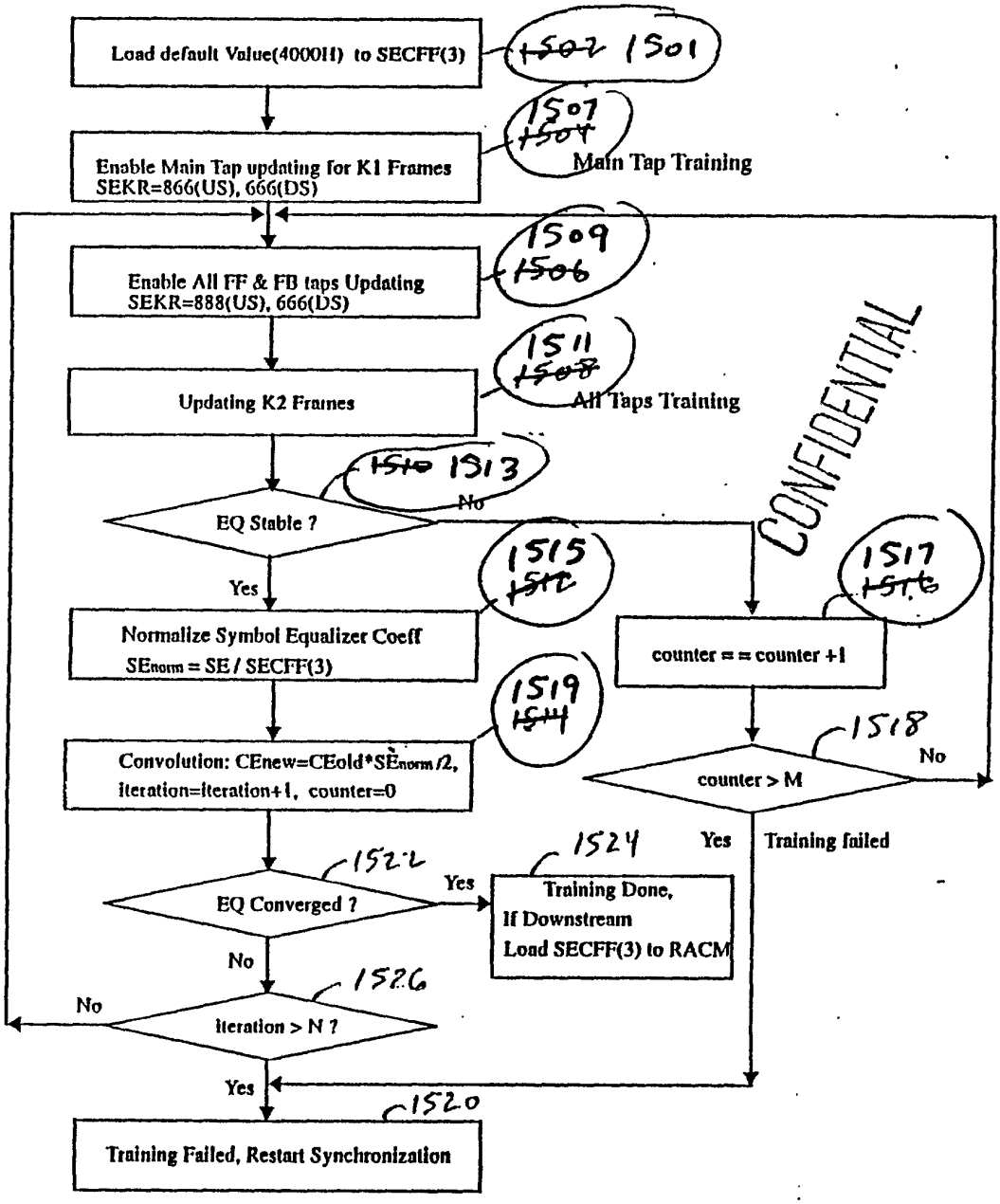
1132

AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND ~~LOADS THESE TAP WEIGHT COEFFICIENTS INTO FFE/DFE CIRCUIT 764~~; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

CONVOLVES THESE SE FILTER TAP WEIGHTS WITH THE OLD FILTER TAP WEIGHTS OF THE FFE AND DFE FILTERS OF CE CIRCUIT 764 AND LOADS THE NEWLY CALCULATED TAP WEIGHTS INTO THE FFE AND DFE FILTERS OF THE CE CIRCUIT

FIG. ~~45C~~ 54C 53C

Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60